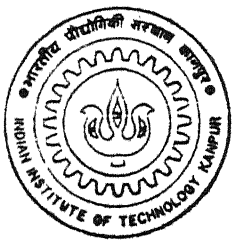
MODELLING OF MOSFET AND POLY-Si TFT

by
ANURAG SAHAI



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for the Degree of

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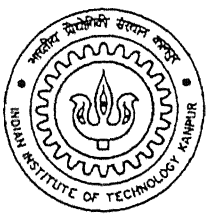
by

ANURAG SAHAI



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CERTIFICATE

It is certified that the work contained in the thesis entitled "*Modelling of MOSFET and Poly-Si TFT*",by *Anurag sahai*, has been carried under my supervision and that this work has not been submitted elsewhere for a degree.

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ABSTRACT

This work presents comprehensive study of MOSFET model. Also presented are models for polysilicon TFT in subthreshold and accumulation regions. The MOSFET model studied enables greater understanding of relatively short-channel ($> 1\mu m$) devices in terms of drain current vs drain voltage characteristics. This model takes into account effect of surface scattering and channel scattering on the carrier mobility. The parameters θ_0 and θ_1 are used to model effects of surface scattering and intrinsic resistance of source and drain region on the carrier mobility, the effects of the parameters η_0 and η_1 account for the effects of lateral field in the channel on the carrier mobility. These effects include the channel velocity saturation. Also presented is a discussion on the extraction of these parameters. The influence of bulk doping on the drain current is described in terms of parameter 'a'.

The subthreshold model for TFT assumes exponential density of states for the gap and expression for differential channel conductance is described and G-V_G characteristics obtained. The model for accumulation region is based on the assumption that the potential barrier height at grain boundary depends on the gate and drain voltage of polysilicon TFT. An effective channel mobility with contribution from grain mobility and boundary mobility is defined and $I_D - V_D$ characteristics of polysilicon TFT is presented.

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Layout Of The Thesis

Chapter. 1. presents introduction of the thesis.

chapter 2 describes theory of MOSFET model including derivations of model equ
In chapter 3. there is discussion of accurate yet simple MOSFET model for enha
mode and depletion mode devices. This chapter uses equations which have been de
chapter 2. Chapter 2 also presents theoretical study of MOSFET model.

Model for subthreshold characteristics of polysilicon Thin-Film Transistors has b
sented in chapter 4.

In chapter 5 modelling of polysilicon Thin-Film-Transistors in accumulation r
presented.

Appendix B presents general mathematical formulations for poly-Si TFT.

Chapter 1

Introduction

Over the years modelling of MOSFET has been used to facilitate the understanding o MOS device. Modelling also enables to consider the various complex effects ,e.g. short c nel effects, influencing the performance of the device. In the analytical models considerat of these effects often becomes unwieldy and assumptions are made to make equations sim such as the assumptions that field is much larger than the lateral field. These assump result in low degree of accuracy in predicting device the characteristics.

In this work, I have considered MOSFET dc model including short channel effects. ther, I have also considered modelling of polysilicon thin film transistor (TFT) whi emerging as an important new technology for large area microelectronics in liquid cr displays and imaging arrays.

1.1 Scope of the Present Work

In this work, modelling of crystalline silicon MOSFET and polycrystalline silicon TFT been considered. The commonly used analytical model used by circuit designers for pre ing MOSFET performance is based on the gradual channel approximation.

This analytical model along with underlying assumption is presented in chapter 2 MOSFET dc model in which several of these assumptions are eliminated is presente short channel device resulting in improvement in accuracy in MOSFET modelling. presented MOSFET model suitable for implementation in circuit analysis has emphas carrier mobility expresssion which includes the effect of surface scattering, channel scatt and substrate bias which include the effects of intrinsic source and drain series resistance

carrier mobility are also included. Polysilicon Thin Film Transistors (TFT) are emergi important new technology for large area microelectronics due to the higher achievable c mobility in polysilicon in comparison to that in a-Si:H. In this work modelling of subthre characteristics of polysilicon TFT is also presented along with model for accumulation re Polysicon TFT based readout electronics has potential application in solid state radi detector for high energy physics and for medical imaging applications.

1.2 Statement of the purpose

Extensive research works have been done in the area of developing analytical formula, bu developed formula is not capable to describe accurate and efficient short channel MOS modelling for I_D-V_D characteristics in the entire region, subthreshold characteristics of Si TFT and accumulation mode of poly-Si TFT . In this thesis, a MOSFET dc n and TFT model is described. In which several modifications have been done to prov significant improvement in accuracy in MOSFET modelling for short channel and po TFT modelling. The presented MOSFET model and poly-Si TFT model is very simple v makes it suitable for implementation in circuit analysis programs. There is discussion MOSFET model with emphasis on a carrier mobility expression which includes the e of surface scattering, channel scattering, and substrate bias. The effects of intrinsic s and drain series resistance on the carrier mobility is also included.

Chapter 2

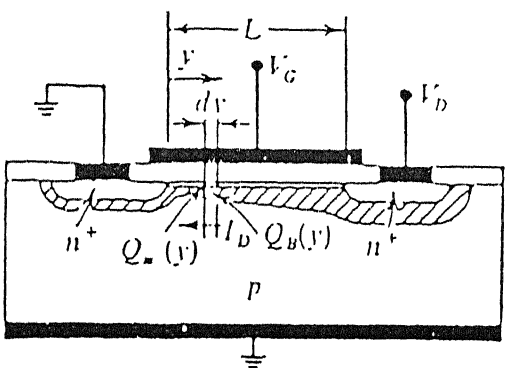
Theory of MOSFET Model

2.1 Current-Voltage Relationship[5]

Let us consider a surface field effect transistor operating in the linear region. The voltag drop across an elemental section of the channel is given by,

$$dV = I_D dR = -\frac{I_D dy}{W \mu_o Q_n(y)} \tag{2.1}$$

Where W is the channel width and $Q_n(y)$ charge density in channel per unit area. At



The elemental section of the channel employed in the derivation of the current-voltage characteristics of surface field-effect transistors.

Figure 2.1 [5]

distance y from the source, the total charge induced in the silicon Q_S will partly consist o

charge in the inversion layer Q_n and partly of charge in the surface depletion region due the ionized acceptor ions, Q_B. Thus,

$$Q_s(y) = Q_n(y) + Q_B(y). \tag{2.}$$

and,

$$V_G - V_{FB} = -\frac{Q_s}{C_o} + \phi_s \tag{2.}$$

which relates the voltage applied to the field plate of an MOS structure to the charge induce in the silicon Q_s and to the surface potential ϕ_s which denotes the total bending of the energ bands. We also include here the flat band voltage V_{FB} which is due partly to the presence charges in the insulator or at the interface, and partly to a finite metal-semiconductor wor function difference as discussed in eq.(2.3). $C_o = \frac{\epsilon_{ox}\epsilon_o}{x_o}$ is the capacitance of the oxide laye per unit area.

Combining these equations (2.2) & (2.3), yields the charge density in the inversion layer,

$$Q_n(y) = -[V_G - V_{FB} - \phi_s(y)]C_o - Q_B(y) \tag{2.4}$$

since it is assumed that a conducting inversion layer exists, the surface potential ϕ_s wi be given approximately by the condition of strong inversion in the presence of an applie voltage.

$$\phi_s(y) = V(y) + 2\phi_f \tag{2.5}$$

Where ϕ_f is the Fermi potential of the substrate, V(y) is the reverse bias between th elemental section of the channel and the substrate. The charge within the surface depletio region Q_B is given by

$$Q_B(y) = -qN_A x_{dmax}(y) = -\sqrt{(2\epsilon_s\epsilon_o qN_A[V(y) + 2\phi_f])}, \tag{2.6}$$

Since the voltage V(y) increases from the source towards the drain due to the IR drop alon the channel, the field-induced junction between the n-type inversion layer and the substrat becomes increasingly reverse biased as it will proceed from source to drain. Hence, both th energy band bending ϕ_s and the charge within the surface depletion region Q_B increase fro source-to drain. Combining above equations 2.1, 2.4, 2.5, 2.6 and integrating equation (2.1 between the source, where y = 0 and V=0, and the drain, where y=L and $V = V_D$, yields

$$I_D = \frac{W}{L}\mu_o C_o\{[V_G - V_{FB} - 2\phi_f - \frac{V_D}{2}]V_D - \frac{2}{3}\frac{\sqrt{(2\epsilon_s\epsilon_o qN_A)}}{C_o}[(V_D + 2\phi_f)^{3/2} - (2\phi_f)^{3/2}]\} \tag{2.7}$$

Which can be written in the form

$$I_D = \frac{W}{L}\mu_o C_o\{[V_G - V_{FB} - 2\phi_f - \frac{V_D}{2}]V_D - \frac{4\epsilon_s x_o}{3\epsilon_{ox} x_{dmax,o}}\sqrt{(2\phi_f)}[(V_D + 2\phi_f)^{3/2} - (2\phi_f)^{3/2}]\} \quad (2.$$

Where

$$x_{dmax,o} = \sqrt{(\frac{2\epsilon_s \epsilon_o (2\phi_f)}{qN_A})} \quad (2.$$

This equation (2.9) is valid only below saturation. Thus the curves shown were calculate for $0 \leq V_D \geq V_{Dsat}$ Beyond V_{Dsat} the current was taken to be constant.

It is interesting to consider the two limiting forms of Equation (2.8). For very small drai voltages, i.e., $V_D << 2\phi_f$, an expansion of the bracketed terms leads to the formulas,

$$I_D \simeq \frac{W}{L}\mu_o C_o[V_G - V_{FB} - 2\phi_f + \frac{Q_{B,o}}{C_o}]V_D \quad (2.10$$

Where

$$Q_{B,o} = -\sqrt{(2\epsilon_s \epsilon_o q N_A (2\phi_f))} \quad (2.11$$

is the charge density per unit area within the surface depletion region, in equilibrium. Thu an ohmic characteristic results. The channel conductance

in the linear region is

$$g = \frac{W}{L}\mu_o C_o (V_G - V_T) \qquad [linear\ region] \quad (2.12$$

Where the threshold voltage V_T, i.e., the voltage that must be applied to the gate in orde to induce a conducting channel, is given by

$$V_T = V_{FB} + 2\phi_f - \frac{Q_{B,o}}{C_o} \quad (2.13)$$

The channel conductance of the MOS transistor in the linear region is a function of gate voltage. The reduction in slope at high gate voltages is due to a decrease in the mobility of electrons owing to increased surface scattering. The above derivation loses its validity when the inversion layer disappears near the drain,i.e., When $V_D = V_{Dsat}$. The condition $Q_n(L) = 0$. yields

$$V_{Dsat} + \frac{\sqrt{(2\epsilon_s \epsilon_o q N_A [V_{Dsat} + 2\phi_f])}}{C_o} + 2\phi_f - V_G + V_{FB} = 0 \quad (2.14)$$

Where it have also used equations 2.5 and 2.6, evaluated at $V = V_{Dsat}$. Solving Equation for V_{Dsat} leads to

$$V_{dsat} = V_G - V_{FB} - 2\phi_f + \frac{\epsilon_s \epsilon_o q N_A}{C_o^2}[1 - \sqrt{(1 + \frac{2C_o^2 (V_G - V_{FB})}{\epsilon_s \epsilon_o q N_A})}] \quad (2.15)$$

or

$$V_{Dsat} = V_G - V_{FB} - 2\phi_f + 4\phi_f(\frac{\epsilon_s x_o}{\epsilon_{ox} x_{dmax,o}})^2[1 - \sqrt{(}1 + (\frac{\epsilon_{ox} x_{dmax,o}}{\epsilon_s x_o})^2 \frac{V_G - V_{FB}}{2\phi_f})]. \quad (2$$

Note that when the oxide thickness x_o is small in comparison to the width of the sur depletion region $x_{dmax,o}$, this expression reduces to the simple form,

$$V_{Dsat} = V_G - V_{FB} - 2\phi_f \qquad [x_o << x_{dmax,o}]. \quad (2$$

subsitution of V_{Dsat} into the current voltage relationship, This equation, gives the magnit of the saturation current, I_{Dsat}.

2.2 Model Equations

Equation (2.7) re-written and modified for body bias has the form

$I_D = \frac{W}{L}\mu_o C_o\{[V_G - V_{FB} - 2\phi_f - \frac{V_D}{2}]V_D - \frac{2}{3}\frac{\sqrt{(2\epsilon_s\epsilon_o qN_A)}}{C_o}[(V_D + 2\phi_f - V_{bs})^{3/2} - (2\phi_f - V_{bs})^{3/2}]\}$

Where $\gamma_o = \mu_o C_o = \frac{\mu_o \epsilon_{ox}\epsilon_o}{t_{ox}}$

and $K = \frac{\sqrt{(2\epsilon_s\epsilon_o qN_A}}{C_o}$.

In the derivation of the models of MOS transistors, following assumptoins are generally made

1.The gradual channel approximation applies.

2.The carrier mobility in the inversion layer is constant.

3.The reverse-biased junction leakage current is negligibly small.

4.The drain current consists of drift current, diffusion current is ignored.

5.In the linear region, the drain-to-source voltage is small compared to $2\phi_f$.

6.Beyond saturation , the drain current is constant.

These assumptions result in a high degree of inaccuracy in predicting current characteristics in short channel devices. It has been found that the following modifications of the above assumptions provide a significant improvement in modelling of these devices.

1)Retention of the entire bulk doping term.

2) Inclusion of the dependence of mobility on gate and drain voltages.

3) Inclusion of intrinsic source and drain series resistance.

4) Inclusion of channel length modulation.

These four effects will be considered in the following sections.

2.3 Bulk Doping Term

The following equation (2.18) for linear region current results from the assumptions previously stated,

$$I_D = \frac{\gamma_o W}{L}[V_{gs} - V_{FB} - 2\phi_f - \frac{V_{ds}}{2}]V_{ds} - \frac{2K}{3}[(V_{ds} + 2\phi_f - V_{bs})^{3/2} - (2\phi_f - V_{bs})^{3/2}] \quad (2.18)$$

It is clear that above equation reduces to

$I_d = \frac{\gamma_o W}{L}[V_{gs} - V_T - \frac{V_{ds}}{2}]V_{ds}$

for $V_{ds} << 2\phi_f - V_{bs}$ For $V_{ds} << 2\phi_f - V_{bs}$, the simple model extends this approximation

results in an improved fit to the measured curves, particularly as the saturation region is approached. To retain the bulk doping term, while including the device threshold voltage in an explicit form for all values of V_{ds}, the following approximation is used. The function

$$F_1(V_{ds}, 2\phi_f - V_{bs}) = \frac{2}{3}[(V_{ds} + 2\phi_f - V_{bs})^{3/2} - (2\phi_f - V_{bs})^{3/2}] \tag{2.19}$$

can be approximated numerically in the range $0 < V_{ds} < 20V$ and $0.6 < 2\phi_f - V_{bs} < 12.6$ by

$$F_1(V_{ds}, 2\phi_f - V_{bs}) = \sqrt{(2\phi_f - V_{bs})}V_{ds} + \frac{0.25g(2\phi_f - V_{bs})}{\sqrt{(2\phi_f - V_{bs})}}V_{ds}^2 \tag{2.20}$$

Where

$$g(2\phi_f - V_{bs}) = 1 - \frac{1}{1.41 + 0.43(2\phi_f - V_{bs})}. \tag{2.21}$$

The detail of this approximation is discussed in sec.(2.6) and (2.7). The drain current in the linear region is given by

$$I_d = \frac{\gamma_o W}{L}[V_{gs} - V_T - a\frac{V_{ds}}{2}]V_{ds} \tag{2.22}$$

Where

$$V_T = 2\phi_f + V_{fb} + K\sqrt{(2\phi_f - V_{bs})} \tag{2.23}$$

and is defined at low V_{ds} as shown,

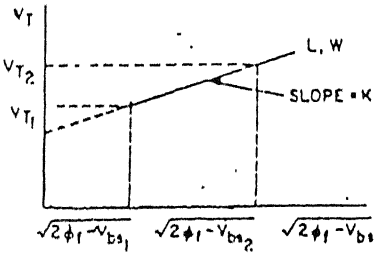


Figure 2.2:

$$a = 1 + \frac{0.5K}{\sqrt{(2\phi_f - V_{bs})}}[1 - \frac{1}{1.41 + 0.43(2\phi_f - V_{bs})}]. \tag{2.24}$$

In the model equations "a" describes the lowering of drain current due to bulk charge in the substrate. The factor "a" given by this equation (2.24) represents the bulk doping effect.

2.4 Carrier Mobility Degradation

Carrier mobility depends on effective normal field E_N and lateral field E_L in the channel. As a first approximation,

$$\mu = \frac{\mu_o}{1 + \alpha|E_N| + \beta|E_L|}. \tag{2.25}$$

If E_1 and E_2 are the electric fields normal to the surface at the $Si-SiO_2$ interface and channel-space charge interface respectively, they may be determined from the following conditions:

$$\epsilon_{si}\epsilon_o(E_1 - E_2) = Q_C \qquad and \qquad \epsilon_{si}\epsilon_o E_2 = Q_B \tag{2.26}$$

where Q_C and Q_B are the channel and bulk charges, respectively. The effective normal electric field in the inversion layer will be

$$|E_N| \simeq E_1 = \frac{Q_B + Q_C}{\epsilon_{si}\epsilon_o} = \frac{C_{ox}}{\epsilon_{si}\epsilon_o}(V_{gs} - 2\phi_f - V_{fb} - V) \tag{2.27}$$

The lateral field E_L is given by

$$|E_L| = \frac{dV}{dY}. \tag{2.28}$$

from these equations, the mobility can be expressed as

$$\mu = \frac{\mu_o}{1 + \theta[V_{gs} - 2\phi_f - V_{fb} - V] + \eta L\frac{dV}{dY}} \tag{2.29}$$

Where

$$\theta = \alpha\frac{C_{ox}}{\epsilon_{si}\epsilon_o}, \tag{2.30}$$

and

$$\eta = \frac{\beta}{L} \tag{2.31}$$

θ and η represent the electric field parameters for surface (normal) scattering and channel (lateral) scattering of carriers in the inversion layer. In order to simplify this expression, it is assumed a constant channel electric field in the lateral direction, i.e.,

$$\frac{dV}{dY} = \frac{V_{ds}}{L}. \tag{2.32}$$

This permits us to average the surface scattering contribution over the channel length as follows:

$$\frac{1}{L}\int_0^L [V_{gs} - V_{fb} - 2\phi_f - V]dy \cong \frac{1}{V_{ds}}\int_0^{V_{ds}} [V_{gs} - V_{fb} - 2\phi_f - V]dV$$
$$= (V_{gs} - V_{fb} - 2\phi_f) - \frac{V_{ds}}{2} = V_{gs} - V_T - \frac{V_{ds}}{2} + K\sqrt{(2\phi_f - V_{bs})} \quad (2.33)$$

With the preceding simplification, the mobility can be expressed as

$$\mu = \frac{\mu_o}{1 + \theta[(V_{gs} - V_T - \frac{V_{ds}}{2}) + K\sqrt{(2\phi_f - V_{bs}] + \eta V_{ds}}} \quad (2.34)$$

The general expression for the current in the linear region is then ($\gamma_o = \mu_o C_{ox}$) modified as,

$$I_d = \frac{\gamma W}{L}[V_{gs} - V_T - a\frac{V_{ds}}{2}]V_{ds} \quad (2.35)$$

where a is defined in equation (2.24) and.

$\gamma = \frac{\gamma_o}{1+\theta(V_{gs}-V_T-\frac{V_{ds}}{2}+K\sqrt{(2\phi_f-V_{bs})+\eta V_{ds}}}$

2.5 Channel Length Modulation

For short channel devices, the drain voltage corresponding to the onset of saturation for a given gate voltage is determined by the requirement that the lateral electric field at the pinch off point is at its critical value E_c. For this field, carriers are at their limiting velocity. To find an expression for the saturation voltage V_{dsat}, we equate the current calculated from the linear portion of the channel with the current at the pinch off point; hence,

$$\mu C_{ox}\frac{W}{L}[V_{gs} - V_T - a\frac{V_{dsat}}{2}]V_{dsat}$$
$$= \mu W C_{ox}[V_{gs} - V_{fb} - 2\phi_f - V_{dsat} - K(V_{dsat} + 2\phi_f - V_{bs})^{1/2}]E_c$$
$$= \mu W C_{ox} F_2(V_{gs}, 2\phi_f - V_{bs})E_c. \quad (2.36)$$

For usual values of voltage, channel length, and thin oxide thickness, we can write with acceptable accuracy.

$$F_2(V_{gs}, 2\phi_f - V_{bs}) =$$
$$V_{gs} - V_{fb} - 2\phi_f - V_{dsat} - K(V_{dsat} + 2\phi_f - V_{bs})^{1/2} = V_{gs} - V_T - aV_{dsat} \quad (2.37a)$$
$$\mu C_{ox}\frac{W}{L}[V_{gs} - V_T - a\frac{V_{dsat}}{2}]V_{dsat}$$

from which we obtain the saturation voltage V_{dsat},

$$V_{dsat} = \frac{V_{gs} - V_T}{a} + E_c L - \sqrt{(\frac{(V_{gs} - V_T)^2}{a^2} + (E_c L)^2)} \tag{2.38}$$

For large values of channel length, $E_c L >> V_{gs} - V_T$, and neglecting the bulk doping effect (a=1), we obtain,

$$V_{dsat} \simeq V_{gs} - V_T. \tag{2.39}$$

The saturation current I_{dsat} is determined by inserting V_{dsat} into equation (2.35) in place of V_{ds}

$$I_{dsat} = \frac{\gamma W}{L}[V_{gs} - V_T - a\frac{V_{dsat}}{2}]V_{dsat}. \tag{2.40}$$

where,

$$\gamma = \frac{\gamma_o}{1 + \theta[(V_{gs} - V_T - \frac{V_{dsat}}{2}) + K\sqrt{(2\phi_f - V_{bs})}] + \eta V_{dsat}} \tag{2.41}$$

Channel length modulation for $V_{ds} > V_{dsat}$, results in the relationship

$$I_d = \frac{\gamma W}{L_I}[V_{gs} - V_T - a\frac{V_{dsat}}{2}]V_{dsat} \tag{2.42}$$

Where derivation of L_I is given below A simplified treatment can be made using the following hypotheses.

1) Mobile carriers have a saturation velocity v_L at the pinchoff point in the channel. The electric field parallel to the surface at this point equals E_c.

2) Mobile carriers between the pinchoff point and the drain are pushed away from the surface by the normal component of the electric field and are collected by the drain diode at the depth x_j. These mobile carriers affect the space charge layer width in the same manner as in the same manner as in the BJT.

3) For the sake of simplicity in the mathematical treatment, we assume that the carriers are spread uniformly in this region over a depth ranging from d for the pinchoff point to x_J for the drain.

Then the set of equations in the drain-channel space charge layer is

$$\frac{\partial^2 V}{\partial y^2} = -\frac{1}{\epsilon_o \epsilon_{si}}(qN_D + \frac{J}{v_L}) \tag{2.43}$$

$$J = \frac{I_{ds}}{Zx} \tag{2.44}$$

$$x = \frac{x_j - d}{l} y + d \tag{2.45}$$

It is assumed, a voltage drop between source and pinchoff point equal to V_{dsat}, and boundary conditions

y=0 at V=V_{dsat}, and $|\frac{dV}{dy}| = E_c \approx \frac{v_L}{\mu_o}$

y=l at V=V_{ds}

From the hypotheses and boundary conditions, the solution for the set of equations (2.43),

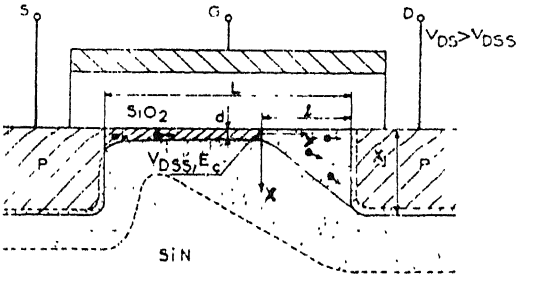
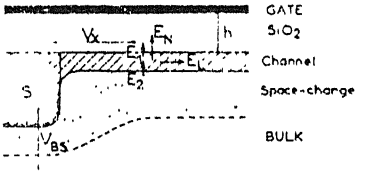


Fig. 1. Section of the MOS transistor.



(2.44) and (2.45) is

Figure 2.3:[9] Normal and lateral fields.

$$V_{ds} - V_{dsat} = \frac{qN_D}{2\epsilon_o\epsilon_{si}} l^2 [1 + \frac{2I_{ds}x_j}{qN_D Z v_L (x_j - d)^2} . (log\frac{x_j}{d} - 1 + \frac{d}{x_j})] + lE_c \qquad (2.46)$$

This formula shows clearly the effect of drain-junction depth x_j on MOS transistor output impedance. If x_j increases, $V_{ds} - Vdsat$ decreases and there is decrease in output impedance. Output impedance is inversely proportional to drain-junction depth and is maximum for $x_j = d$.

For the usual diffusion , $x_j >> d$ and (2.46) gives

$$V_{ds} - V_{dsat} = \frac{qN_D}{2\epsilon_o\epsilon_{si}} l^2 [1 + \frac{2I_{ds}}{qN_D Z v_L x_j} . (log\frac{x_j}{d} - 1)] + lE_c \qquad (2.47)$$

subsitute $A = \frac{qN_D}{2\epsilon_o\epsilon_{si}}$, $B = \frac{2(log\frac{x_j}{d} - 1)}{qNv_L WD_j}$ and $V_c = E_c L$

$$0 = A/L^2 l^2 [1 + BI_{ds}] + 2V_c/L - 2(V_{ds} - V_{dsat}) \qquad (2.48)$$

$$l = L(\frac{-2V_c \pm \sqrt{(4V_C{}^2 + 8A(1 + BI_{ds})(V_{ds} - V_{dsat}))}}{2A(1 + BI_{ds})}) \qquad (2.49)$$

$= L-1$

$$L_I = L - L\frac{[V_c^2 + 2A(1+BI_{dsat})(V_{ds} - V_{dsat})]^{1/2} - V_c}{A(1+BI_{dsat})}. \tag{2.50}$$

e mobility modulation factor θ factor consists of two parts. The first part, θ_o, is caused by conventional mobility degradation due to surface scattering of carriers in the inversion er. The second part, θ_1/L, is interpreted to be the effect of intrinsic series resistance r_i in source or the drain on the apparent mobility . The η factor also consists of two parts. e η_o part is believed to exit due to the approximations used in deriving the mobility endence on V_{ds}, and its value is very close to zero. The second part, η_1/L, is due to nnel velocity saturation effects (channel scattering of carriers in the inversion layer).

2.6 Effect Of Intrinsic Source AND/OR Drain Series Resistance On The Carrier Mobility

The parameter θ_1 is caused by the device "intrinsic" resistance r_i that is due to current crowding in the drain-to-source and drain to channel regions. The results are valid for all values of V_{ds}. Linear relationship (For$V'_{ds} << V_{gs} - V_T$ and $V_{gs} > V_T$)

$$I_d = \frac{\gamma_O W}{L}[V_{gs} - V_T]V'_{ds}, \tag{2.51}$$

where,

$$V'_{ds} = V'_d - V'_s, \tag{2.52}$$

$$V'_d = V_d - I_d\frac{r_i}{2}, \tag{2.53}$$

and

$$V'_s = I_d\frac{r_i}{2}. \tag{2.54}$$

To simplify these equations, we get

$$V'_{ds} = V_{ds} - I_d r_i. \tag{2.55}$$

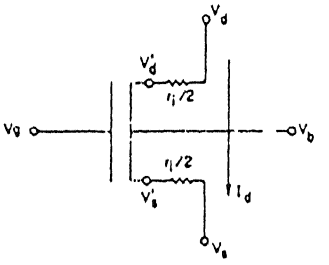
in terms of V_{ds} and V_{gs},

$$I_d = \frac{\gamma_0}{1 + \frac{\theta_1}{L}(V_{gs} - V_T)}\frac{W}{L}[V_{gs} - V_T]V_{ds}, \tag{2.56}$$

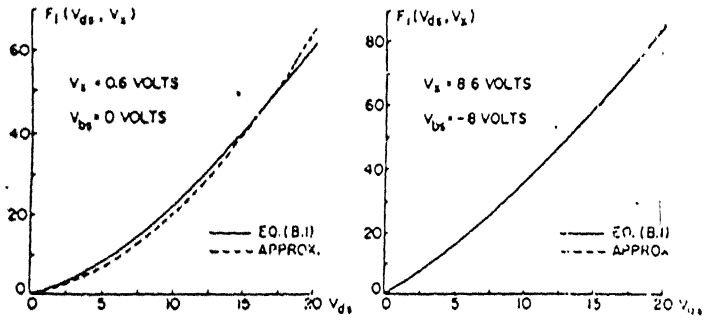
where θ_1 is defined as

$$\theta_1 = \gamma_0 W r_i = constant.\gamma_0. \tag{2.57}$$

Since r_i is proportional to 1/W,this imply that θ_1 is independent to W and θ_1 is only dependent of γ_0.



Intrinsic source and drain series resistances.



Approximating $F_1(V_{ds}, 2\phi_f - V_{bs})$.

2.7 Numerical Approximation Of Function $F_1(V_{ds}, 2\phi_f - V_{bs})$

The accurate approximation of function over a reasonable range of V_{ds} and $2\phi_f - V_{bs}$.Let

$$V_x = 2\phi_f - V_{bs}. \tag{2.58}$$

For small V_{ds},

$$F_1(V_{ds}, V_X) = \frac{2}{3}[(V_{ds} + V_X)^{3/2} - (V_X)^{3/2}] \tag{2.59}$$

by expanding it,

$$F_1(V_{ds}, V_X) = (V_X)^{1/2}V_{ds} + 0.25(V_{ds})^2/(V_X)^{1/2} + ... \tag{2.60}$$

This expansion is valid for only $V_{ds} << V_X$. The expansion is modified to

$$F_1(V_{ds}, V_X) = (V_X)^{1/2}V_{ds} + \frac{0.25(V_{ds})^2 g(V_X)}{(V_X)^{1/2}} \tag{2.61}$$

Where $g(V_X)$ is determined by expanding this equation to give the best fit to $F_1(V_{ds}, V_X)$ over the desired voltage range. The parameter g for each fixed V_X is determined the expression $(V_X)^{1/2}V_{ds} + 0.25\frac{(V_{ds})^2 g}{(V_X)^{1/2}}$. can be accurately approximated by

$$g = 1 - \frac{1}{P_1 + P_2 V_X} \tag{2.62}$$

Where P_1 and P_2 are determined by linear squares fitting over the range of V_X. The result is $P_1 = 1.408$ *and* $P_2 = 0.4333$.

2.8 Numerical Approximation of Function $F_2(V_{gs}, 2\phi_f - V_{bs})$

To find a good approximation of $F_2(V_{gs}, 2\phi_f - V_{bs})$ over the usual values of voltages .Assume, $F_2 = 2\phi_f - V_{bs}$. Hence,

$$\begin{aligned} F_2(V_{gs}, V_X) &= V_{gs} - V_{fb} - V_{dsat} - K(V_{dsat} + V_X)^{1/2} - 2\phi_f \\ &= V_{gs} - V_{fb} - 2\phi_f - V_{dsat} - K\sqrt{V_X}[1 + \frac{V_{dsat}}{V_X}]^{1/2} \end{aligned} \tag{2.63}$$

Expanding the factor $[1 + \frac{V_{dsat}}{V_X}]^{1/2}$ using Taylor series and taking first and second term only,

2.8 Subthreshold Region

When gate voltage is below the threshold voltage and the semiconductor surface in weak inversion, the corresponding current is called the subthreshold current. In weak inversion, the drain current (dominated by diffusion),

$$I_D = -qAD_n\frac{dn}{dy} = qAD_n\frac{n(0)-n(L)}{L} \tag{2.63}$$

where A is the cross section of the curernt flow, and n(0) and n(L) are the electron densities in the channel at the source and the drain, respectively. These electron densities are given by,

$$n(0) = n_{po}e^{\beta\psi_s} \tag{2.64}$$

$$n(L) = n_{po}e^{\beta\psi_s-\beta V_D} \tag{2.65}$$

where ψ_s is the surface potential at the source. The weak inversion surface field E_s is given by,

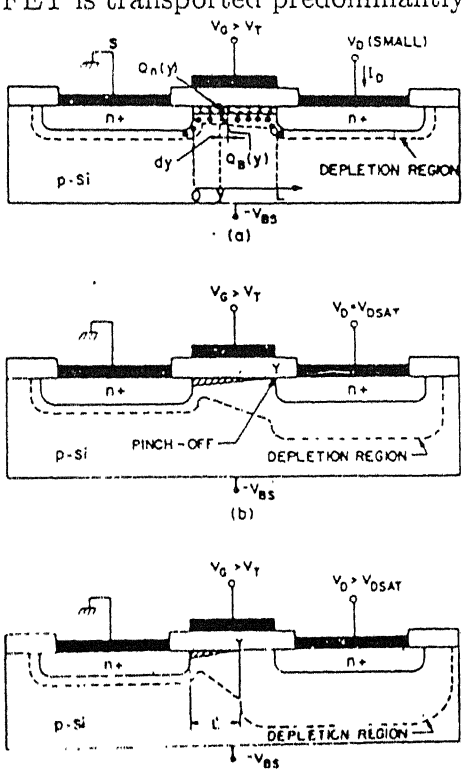
$$E_s = -Q_B/\epsilon_s = \sqrt{2qN_A\psi_s/\epsilon_s} \tag{2.66}$$

Subsituting Eqs. 2.64, 2.65 into 2.63 gives

$$I_D = \mu_o(\frac{W}{L})\frac{aC_j}{2\beta^2}(\frac{n_j}{N_A})^2(1-e^{-\beta V_D})e^{\beta\psi_s}(\beta\psi_s)^{-1/2} \tag{2.67}$$

Where q is the electronic charge; μ_o is the effective electron mobility; L is the channel length; W is the transistor width; The Schematic diagram of a MOSFET is shown below,

Because the current in a MOSFET is transported predominantly by carriers of one polarity



only (e.g., electrons in an n-channel device), the MOSFET is usually referred to as a unipolar device. The MOSFET is a member of the family of field effect transistors. Although MOSFETs have been made with various semiconductors , the most important system is the $Si - SiO_2$ combination. We first consider the basic device charactristics of the so called long channel MOSFET; that is, the channel length L is much longer than the sum of the source and drain depletion layer widths $(W_s + W_D)$. This serves as a foundation to understand short channel, that is,$L <= (W_S + W_D)$, and related MOSFET devices. For short channel devices, the full effect of Q_B on the threshold voltage is reduced, because near the source and drain ends of the channel, some field lines originating from the source or drain terminate at the bulk charges in the channel region for $V_D = 0$. For $V_D > 0$,the depletion region near the drain expands further . Note that the horizontal depletion layer widths y_s and y_D are smaller than the vertical depletion layer widths W_S and W_D, respec tively, because the transeverse field strongly influences the potential distri bution at the surface.

Because of the reduction of the bulk charge Q_B, surface potential for a given gate voltage increases, leading to an increase of subthreshold current . The surface potential can be found from the following expression:

$$V_G - V_{FB} = \psi_s + \frac{1}{C_i}\sqrt{(q\epsilon_s N_A(\psi_s + N_A(\psi_s + V_{BS})/2))}(1 + \frac{L - W_D - W_S}{L - y_D - y_s}) \tag{2.68}$$

where W_D and W_S are given,

$$W_D = \sqrt{(\frac{2\epsilon_s}{qN_A}(V_D + V_{bi} + V_{BS}))} \qquad \mu m \tag{2.69}$$

W_S can be get by putting V_D=0,

$$W_S = \sqrt{(\frac{2\epsilon_s}{qN_A}(V_{bi} + V_{BS}))} \tag{2.70}$$

$$y_S = \sqrt{(\frac{2\epsilon_s}{qN_A}(V_D + V_{bi} + V_{BS})} \tag{2.71}$$

$$y_D = \sqrt{(\frac{2\epsilon_s}{qN_A}(V_{bi} - \psi_s))} \tag{2.72}$$

The subthreshold current is given by

$$I_D = \mu_o(\frac{W}{L - y_s - y_D})\frac{aC_j}{2(\beta)^2}(\frac{n_j}{N_A})^2(1 - \exp(-\beta V_D)\exp(\psi_s)(\beta\psi_s)^{1/2} \tag{2.73}$$

Equation (2.73) is identical to equation (2.67), except channel length is replaced by the effective channel length:

$$L_{eff} = L - y_s - y_D. \tag{2.74}$$

Chapter 3

The MOSFET Model

3.1 The Model

The model equations are derived — in chapter 2.

3.1.1 Saturation Voltage-V_{dsat}

The saturation voltage given by eq. 3.1 below is used to determine whether a device is in the linear or saturated region. The equation is derived in chapter 2 (eq.(2.38))

$$V_{dsat} = \frac{V_{gs} - V_T}{a} + V_C - \sqrt{((\frac{V_{gs} - V_T}{a})^2 + V_C^2)} \tag{3.1}$$

Where

V_{gs}= gate-to-source voltage.

V_{ds}= drain-to-source voltage.

V_{bs}= bulk (or substrate)-to-source voltage.

V_T= $V_T(L, W, V_{ds})$ is the device threshold voltage. For small value of V_{ds} can be ($\leq$100mv), V_T can be determined.

$$V_c = E_c L = \frac{v_l}{\mu_0} L \tag{3.2}$$

$$\mu_o = \frac{\gamma_o t_{ox}}{\epsilon_o \epsilon_{ox}} \tag{3.3}$$

E_c critical field in the channel (for this field, carriers are in their limiting velocity v_L) in V/cm.

μ_o carrier mobility at low gate and drain fields in cm^2/V.s.

channel length (wafer) in cm.

V channel width (wafer) in cm.

$_o$ gain factor in $\mho$/V.

$_{ox}$ oxide thickness in cm.

, permittivity of free space in F/cm.

$_{ox}$ relative permittivity of SiO_2.

$_s$ relative permittivity of Si; and

'his equation 3.4 has been derived in chapter 2(eq.2.24).

$$a = 1 + \frac{0.5K}{\sqrt{(2\phi_f - V_{bs})}}[1 - \frac{1}{1.41 + 0.43(2\phi_f - V_{bs})}] \quad (3.4)$$

'here

: slope of V_T versus $\sqrt{(2\phi_f - V_{bs})}$ curve. Equation for K is derived in chapt. 2. As is vident from eq.(2.23)

$_T = 2\phi_f + V_{fb} + K\sqrt{(2\phi_f - V_{bs})}$.

'hus,

$$K = \frac{V_{T2} - V_{T1}}{\sqrt{(2\phi_f - V_{bs2})} - \sqrt{(2\phi_f - V_{bs1})}} \quad (3.5)$$

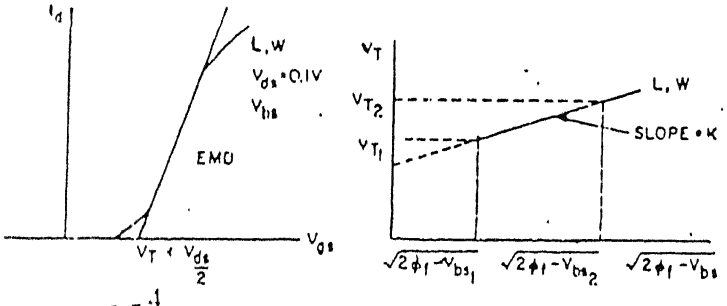


Fig.3.1 Interpretation of model parameter.

$_{T1}, V_{T2}, V_{bs1}$, and V_{bs2} are as shown in fig.(3.1).

$2\phi_f$ twice the Fermi potential level in the "bulk" $2\phi_f = 0.6$V for bulk doping of 1.2e15 cm^{-}3. The value of K is dependent on the doping profile. For uniform doping, in more practical ase when threshold tailoring results in nonuniform doping, K may be treated as a constant o a good approximation over the voltage range of interest ($V_{ds} \leq -1.5$ and $V_{ds} \geq 0V$).

3.1.2 Linear Region

$0 \leq V_{ds} < V_{dsat}$ and $V_{gs} >= V_T$. From chapter 2(eq.2.35)

$$I_d = \frac{\gamma W}{L}[V_{gs} - V_T - a\frac{V_{ds}}{2}]V_{ds} \tag{3.6}$$

where, equation for γ has been taken from chapter 2 (eq.(2.41)).

$$\gamma = \frac{\gamma_o}{1 + \theta(V_{gs} - V_T - \frac{V_{ds}}{2} + K\sqrt{(2\phi_f - V_{bs})} + \eta V_{ds}} \tag{3.7}$$

Equation for η and β ,

$$\theta = \theta_o + \frac{\theta_1}{L}; \tag{3.8}$$

$$\eta = \eta_o + \frac{\eta_1}{L}; \tag{3.9}$$

3.1.3 Saturation Region

$V_{ds} > V_{dsat}$ and $V_{gs} >= V_T$

$$I_d = \frac{\gamma W}{L_I}[V_{gs} - V_T - a\frac{V_{dsat}}{2}]V_{dsat} \tag{3.10}$$

where

$$L_I = L - L\frac{[V_c^2 + 2A(1 + BI_{dsat})(V_{ds} - V_{dsat})]^{1/2} - V_c}{A(1 + BI_{dsat})}. \tag{3.11}$$

$$A = \frac{qNL^2}{\epsilon_o \epsilon_{si}} \qquad (V). \tag{3.12}$$

$$B = \frac{2(log\frac{\mathcal{X}_j}{d} - 1)}{qN v_L W D_j} \qquad (A)^{-}1. \tag{3.13}$$

q=electron charge.

N=impurity density at the drain space charge region.

$\mathcal{X}_j$=junction depth(cm).

d=mean inversion layer thickness (cm).

$$v_c = \frac{v_L}{\mu_o}L. \tag{3.14}$$

$$\gamma = \frac{\gamma_o}{1 + \theta[(V_{gs} - V_T - \frac{V_{dsat}}{2}) + K\sqrt{(2\phi_f - V_{bs})}] + V_{ds}\eta} \tag{3.15}$$

$$\theta = \theta_o + \frac{\theta_1}{L_I}. \tag{3.16}$$

$$\eta = \eta_o + \frac{\eta_1}{L_I}. \tag{3.17}$$

3.1.4 Cut off Region

$$V_{gs} < V_T. \tag{3.18}$$

$$I_d = 0. \tag{3.19}$$

The model parameters γ_o, K, θ and η obey certain relationships with physical parameters as are explained in the following. γ_o is the gain factor and is related to the physical parameters by the relationship

$$\gamma_o = \mu_o C_{ox} \tag{3.20}$$

where

C_{ox} is the oxide capacitance per unit area in F/cm^2.

It is emphasized that the mobility modulation factors θ and η modify γ according to model equation (3.15). The factor "a" describes the lowering of the drain current due to bulk charge in the substrate according to eq.(3.10). The effect of current modulation due to the short and narrow channel effects is embedded in the model parameter K. Note that when a is set to 1 and θ and η are set to 0,

$$I_d = \gamma_o \frac{W}{L}[V_{gs} - V_T - \frac{V_{ds}}{2}]V_{ds} \qquad for 0 <= V_{ds} < V_{dsat} \tag{3.21}$$

and

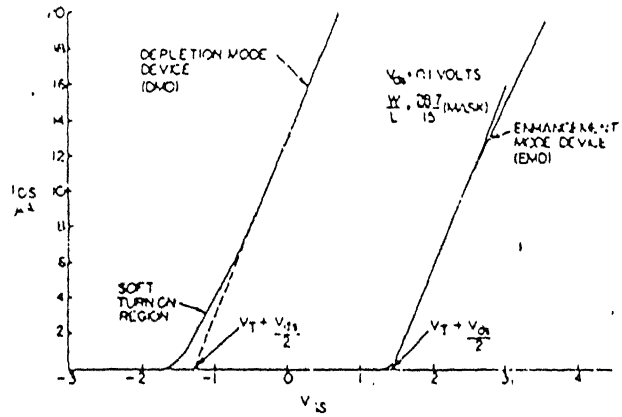
$$I_d = \frac{\gamma_o W}{2L}[V_{gs} - V_T]^2 \qquad for V_{ds} >= V_{dsat}, \tag{3.22}$$

Which are the classical equations for a simple MOSFET model.

3.2 For Depletion Mode

The turn on characteristics, I_{ds} versus V_{gs} measured with a small drain voltage, are shown here for enhancement and depletion devices with the same physical dimension. A threshold value V_T of gate voltage is defined by matching the experimental curve to a straight line segment asymptotically at the region of maximum slope, extrapolated to zero current, intersecting the axis at $V_T + V_{ds}/2$, from which V_T is determined. When the gate voltage is

below $V_T + V_{ds}$, the device is in pinchoff, and the current varies as $(V_{gs} - V_T)^2$ according to the simple theory. The depletion device behaves somewhat differently in this "soft turn-on region" and has a definite (but small) current level at $V_{gs} = V_T$ due to subsurface conduction in the implanted n-type layer. The straight line segment matches the depletion device current very well at $V_{gs} = 0$, which is the usual bias condition for a depletion type load device in standard logic circuits, so this threshold definition is meaningful for modelling such circuits. The slopes of the straight line segment are similar for enhancement and depletion mode devices.



Turn-on characteristics of EMD and DMD devices showing threshold definitions.

Figure 3.II [4]

The current behaves of the depletion mode devices with shallow implanted channels can be adequately described by 3.1-3.17 equations, which represent an enhancement surface channel device when defining the depletion device threshold V_T as explained above. The turn-on characteristics, $I_{ds} vs V_{gs}$ measured with a small drain voltage, are shown in fig.(3.II).

3.3 Extracting Model Parameters

A parameter extraction method for the above model is described below. It uses conventional methods to extract V_T and K, and uses a linear technique to extract $\gamma_o, \theta_o, \theta_1, \eta_o$, and η_1.

The measured data were taken from reference (4) in Bibliography with bias voltage of V_{bs} from -1.5 to 8 V, V_{gs} from 0.5 to 4 V above $|V_T|$, and V_{ds} from 0 to 5 V. For enhancement mode devices with channel lengths from 1.0 to 13 μm, channel widths from 2 to 27 μm, substrate doping = $1.2e15cm^3$ oxide thickness = 45nm, and junction depth = 0.5 μm. The saturation velocity v_L for electrons was assumed = $15e6cm/s$ and the mean inversion layer thickness d was assumed to be 10 nm. For small values of $V_{ds}(= 0.1V)$ and large values of $V_{gs}(V_{gs} - V_T) >> K\sqrt{(2\phi_f - V_{bs})}$,

$$I_d = \frac{\gamma_o W}{L} \frac{(V_{gs} - V_T - \frac{V_{ds}}{2})}{1 + \theta(V_{gs} - V_T - \frac{V_{ds}}{2})} V_{ds}. \tag{3.23}$$

This also can be reduces in this form,

$$R_{ds} = \frac{V_{ds}}{I_d} = \frac{1}{\beta_0}(\frac{1}{V_{gs} - V_T - \frac{V_{ds}}{2}} + \theta) \tag{3.24}$$

where

$$\beta_o = \frac{\gamma_o W}{L} \tag{3.25}$$

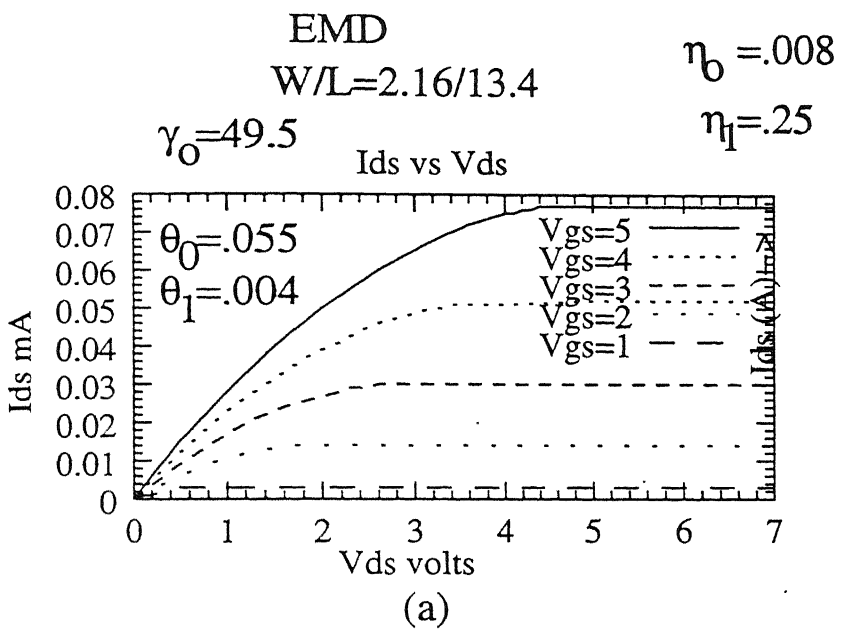
(The programme for MOSFET is presented in sec.C.1 of Appendix C.)

3.4 Results

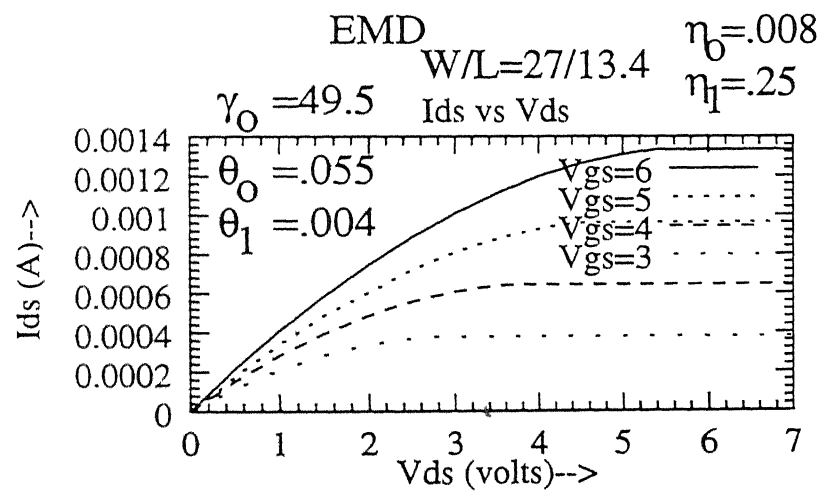
The MOSFET model for short channel is described above. The drain current I_{DS} is ploted against V_{ds} for different regions or different conditions which are dependent on the values of V_{gs} and V_T. Fig.3.1. 3.2. 3.3. 3.4 shows the drain current characteristics using this model.
Fig.3.1(a) and (b) shows comparison of drain current and drain voltage characteristics in enhancement mode device for constant θ_0 and different channel widths.
Fig.3.2(a) and (b) shows comparison of drain current and voltage characteristics in enhancement mode device for constant channel length, channel width and different θ_0.
Fig.3.3(a) and (b) shows comparison of drain current and voltage characteristics in depletion mode device for constant θ_0. channel width and different channel lengths.
Fig.3.4(a) and (b) shows comparison of drain current and voltage characteristics in depletion mode device for constant θ_0 and different channel lengths and widths.
The slope of the line $\frac{V_{ds}}{I_{ds}}$ versus $[\frac{1}{V_{gs}-V_T-\frac{V_{ds}}{2}}]$ represents $\frac{1}{\beta_o}$ and y-intercept shows $\frac{\theta}{\beta_o}$. This is shown in fig. 3.5 (a). Family of these curves give values $\frac{1}{\beta_0}$ and $\frac{\theta}{\beta_0}$.
To plot $\frac{1}{\beta_o}$ versus L_m, it is found that slope of this line is equal to $\frac{1}{\gamma_0 W}$ and the x-intercept is equal to ΔL. where ΔL =Design channel length -Actual channel length . This is shown in fig.3.5(b) for neighbouring transistors with constant W and different L.
ΔW is determined by the measure of x-intercept of the line drawn between β_o and W_m. This is shown in fig.3.6(a). Fig.3.6(a) is β_0 vs W with x-intercept, where ΔW= design channel width. -actual channel width.
Fig.3.6(b) is a plot of the line $\frac{V_{ds}}{I_{ds}}$ versus $[\frac{1}{V_{gs}-V_T-\frac{V_{ds}}{2}}]$ for constant length and different widths. The slope of these lines is $\frac{1}{\beta_0}$ and y-intercept is $\frac{\theta}{\beta_0}$.

The θ_o is determined as the slope of the line which is drawn between $\frac{\theta}{\beta_o}$ and $\frac{1}{\beta_o}$ and y-intercept is equal to $r_i + R_s$. This is shown in fig.3.7(a).
Fig.3.7(b) is a plot of η versus β_0 and slope of this plot gives the value of $\frac{\eta_1}{\gamma_0 W}$.
Information obtained from fig.3.5(a) is used in fig.3.7(b) i.e. $\frac{1}{\beta_0}$ and $\frac{\theta}{\beta_0}$ where $\frac{\theta}{\beta_0}$ vs $\frac{1}{\beta_0}$ is plotted in fig.3.7(a) the y-intercept gives $r_i + R_s$ where R_s is the parasitic resistance in the source or the drain and θ_0 is the slope of the line. Plot of η vs β_0 shown in fig. 3.7(b) is a straight line with extrapolated intercept gives η_0. η_1 is obtained from the slope.
There is good agreement between measured and calculated data. In this model, a parameter extraction method has been used to extract $\gamma_0, \theta_0, \eta_0$ and η_1. It has been found that the ac

curate of the simple MOSFET current model can be significantly improved by including the effects of the entire bulk doping term, the dependence of carrier mobility on gate voltage, drain voltage. intrinsic source and drain series resistance and channel length modulation. Also shown is detailed derivation of the model equations and a method of extracting model parameter.



(a)



(b)

D_j =0.5 μ m

$n = 1.2 \times 10^{15} cm^{-3}$

V_{t1}= 80 mV

I_{dsat} = 1 mV

V_{t2} = 40mV

V_T = 45 mV

V_{bs} = -3 Volts

$v_l = 15 \times 10^6$ cm /s

d = 10 nm

t_{ox} = 45nm

ϕ_f = 0.3 V

V_{bs2} = -8.0V

V_{bs1} = -1.5 V

Figure 3.1: (a)-(b)$I_d vs V_{ds}$ characteristics of MOSFET for different widths

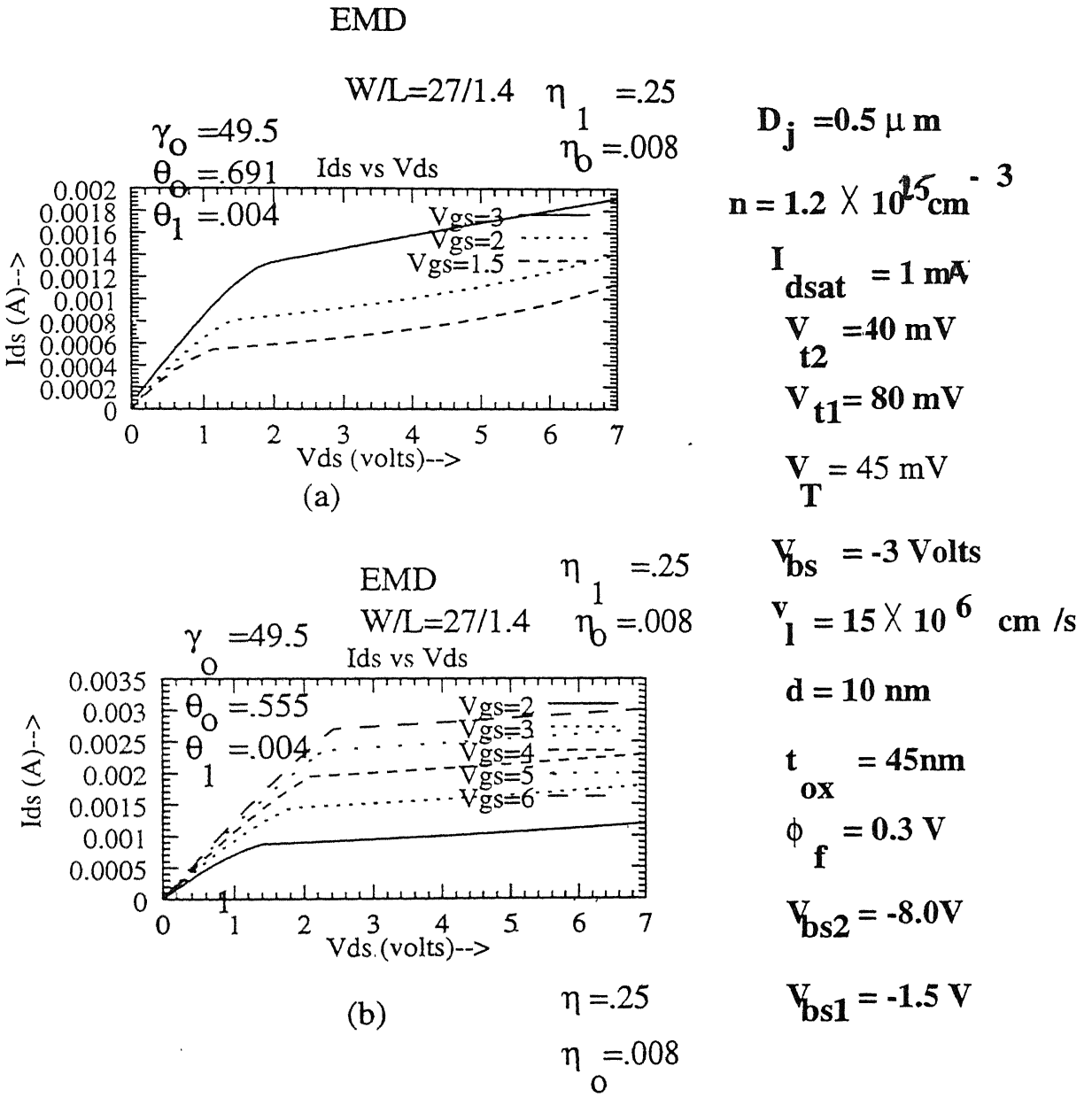


Figure 3.2: (a)-(b)$I_d vs V_{ds}$ char acteristics of MOSFET for different parameter θ_o

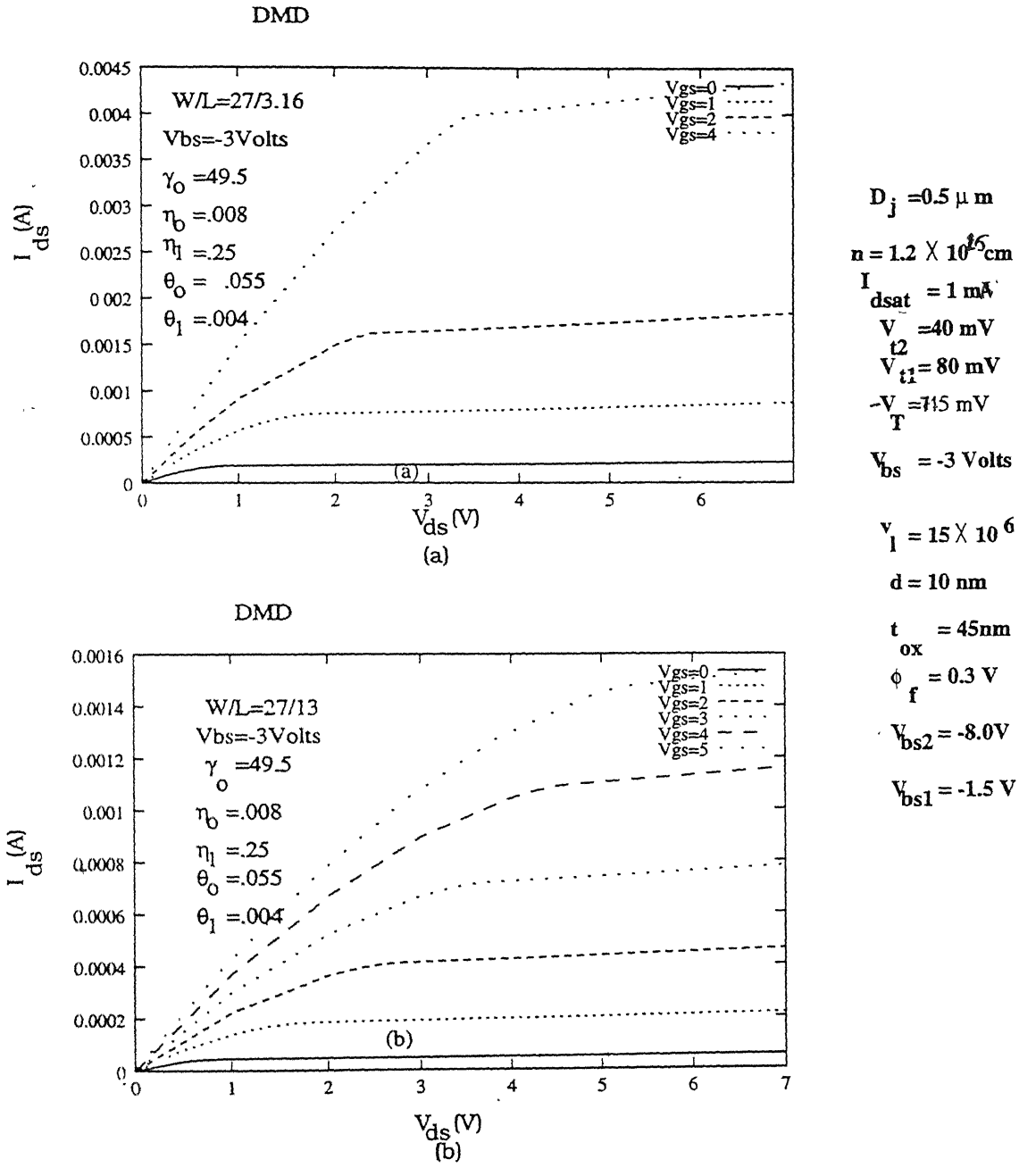


Figure 3.3: (a)-(b)$I_d vs V_{ds}$ char acteristics of MOSFET for different lengths

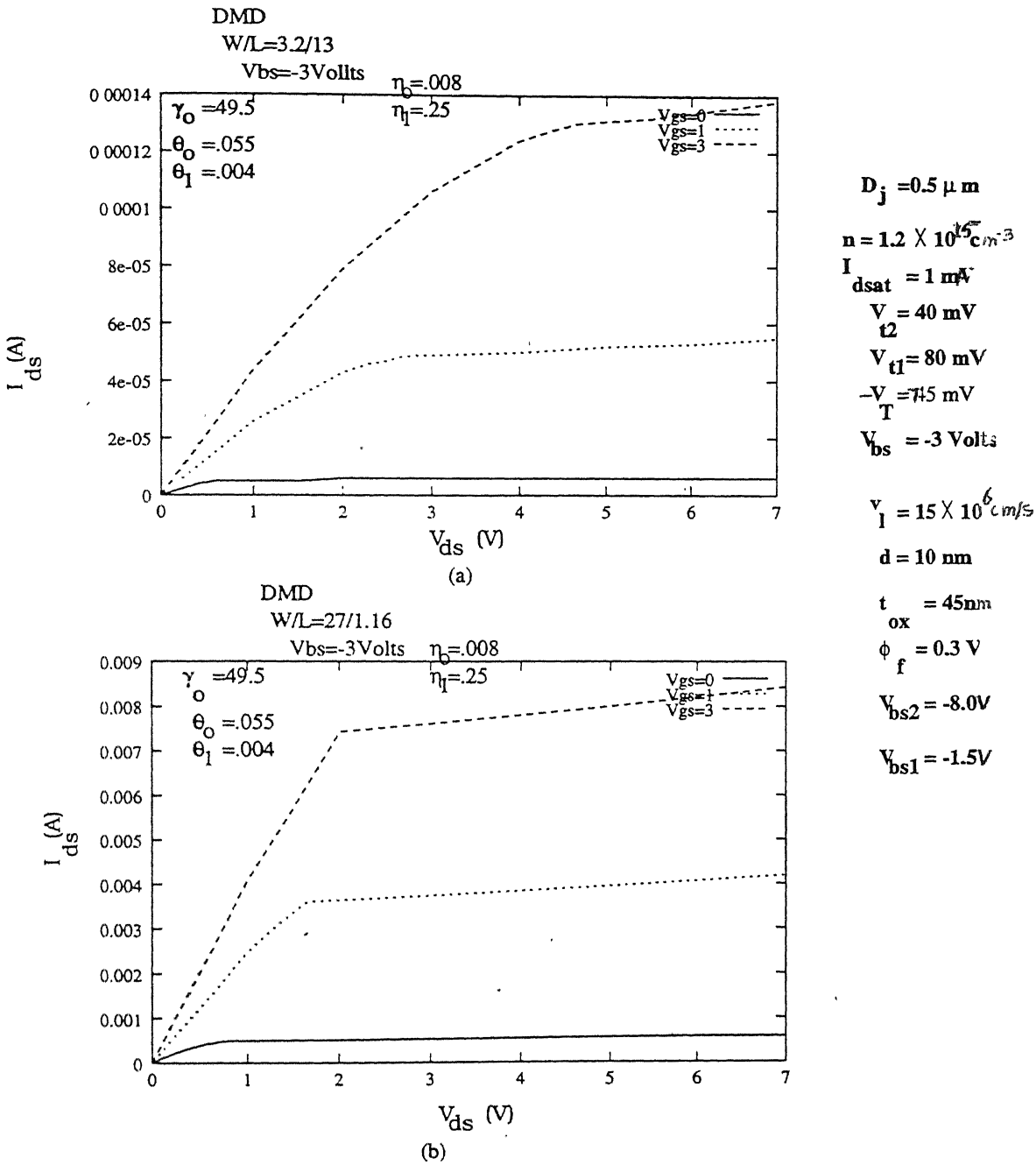
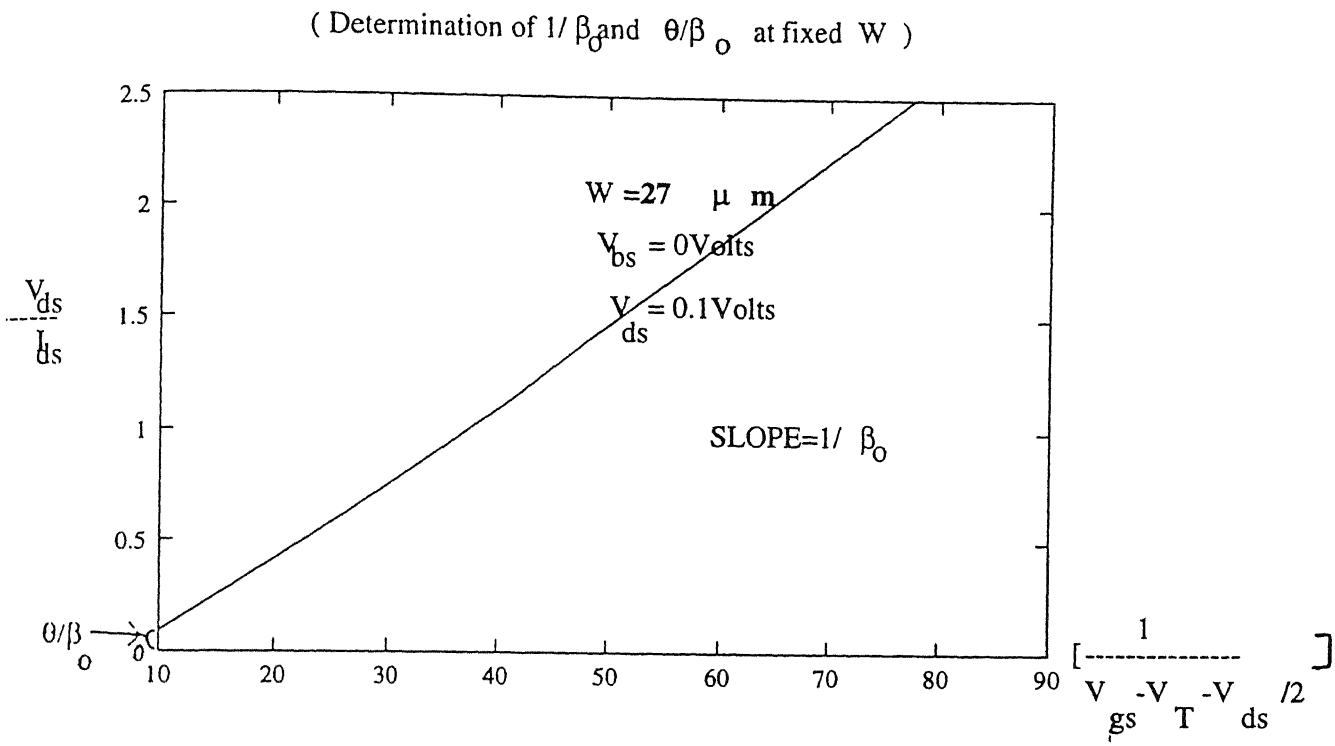
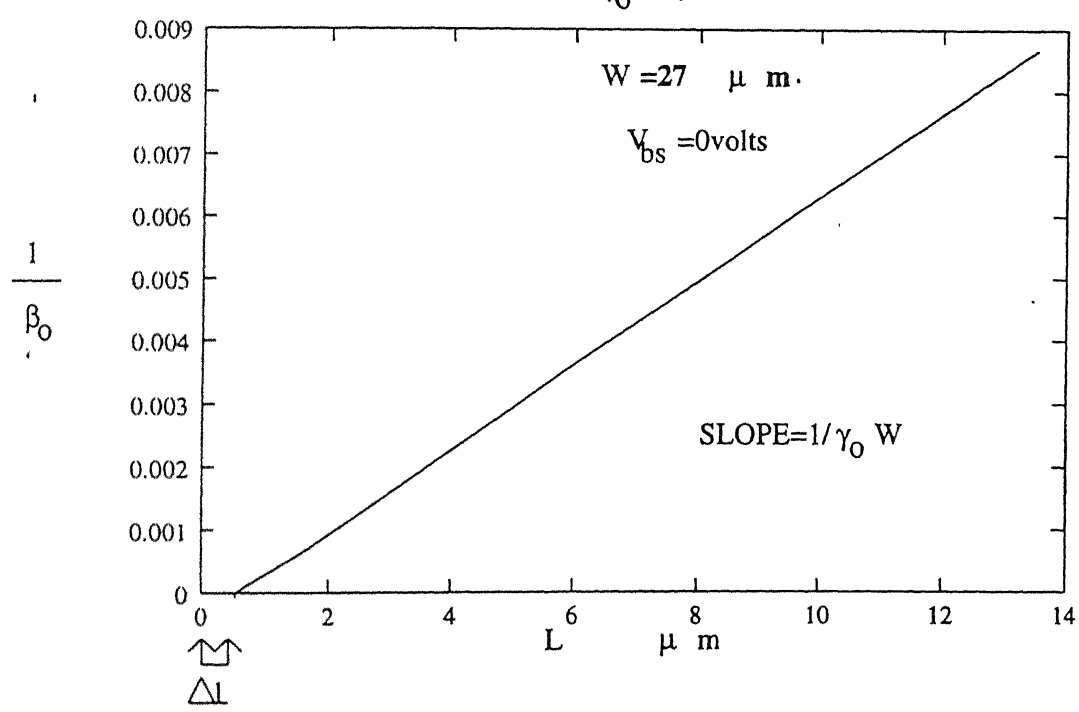


Figure 3.4: (a)-(b)$I_d vs V_{ds}$ char acteristics of MOSFET for different widths and lengths



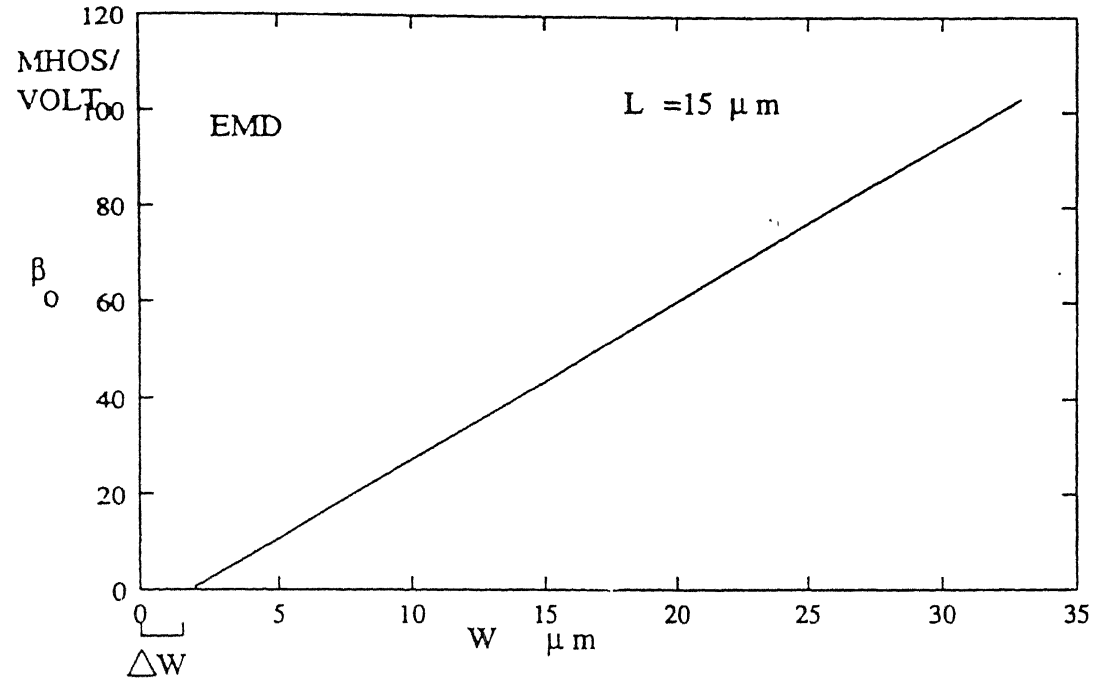
(b) Plot of $\frac{V_{ds}}{I_{ds}}$ vs $\left[\frac{1}{(V_{gs}-V_T-V_{ds})/2}\right]$



(a) Plot of $1/\beta_o$ vs L

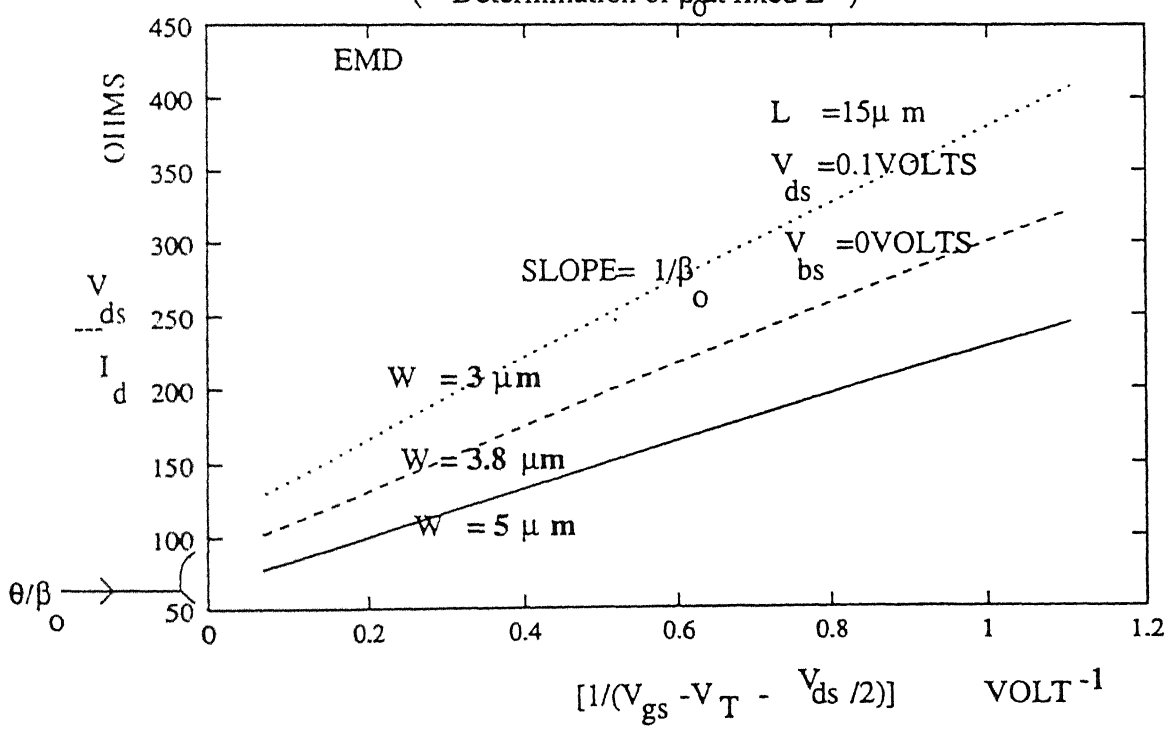
Figure 3.5: (a)-(b)

(Determination of ΔW)



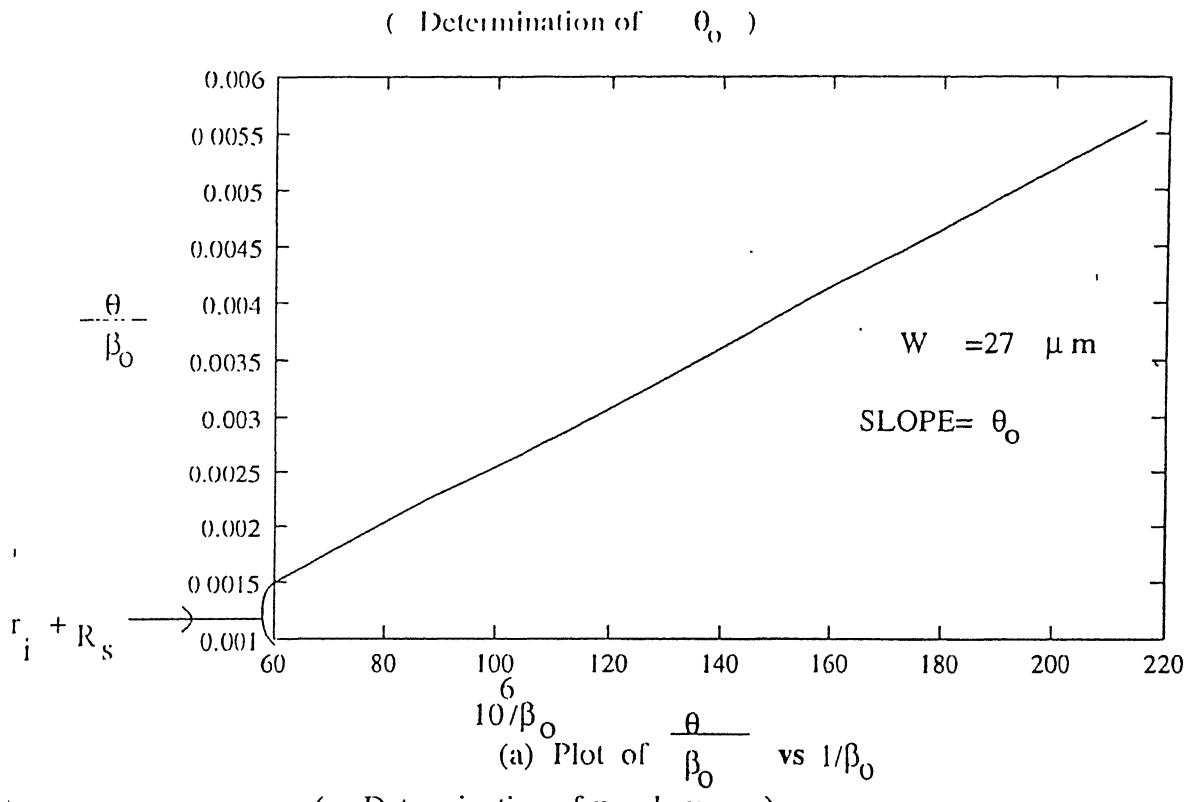
(a) Plot of β_o vs W

(Determination of β_o at fixed L)

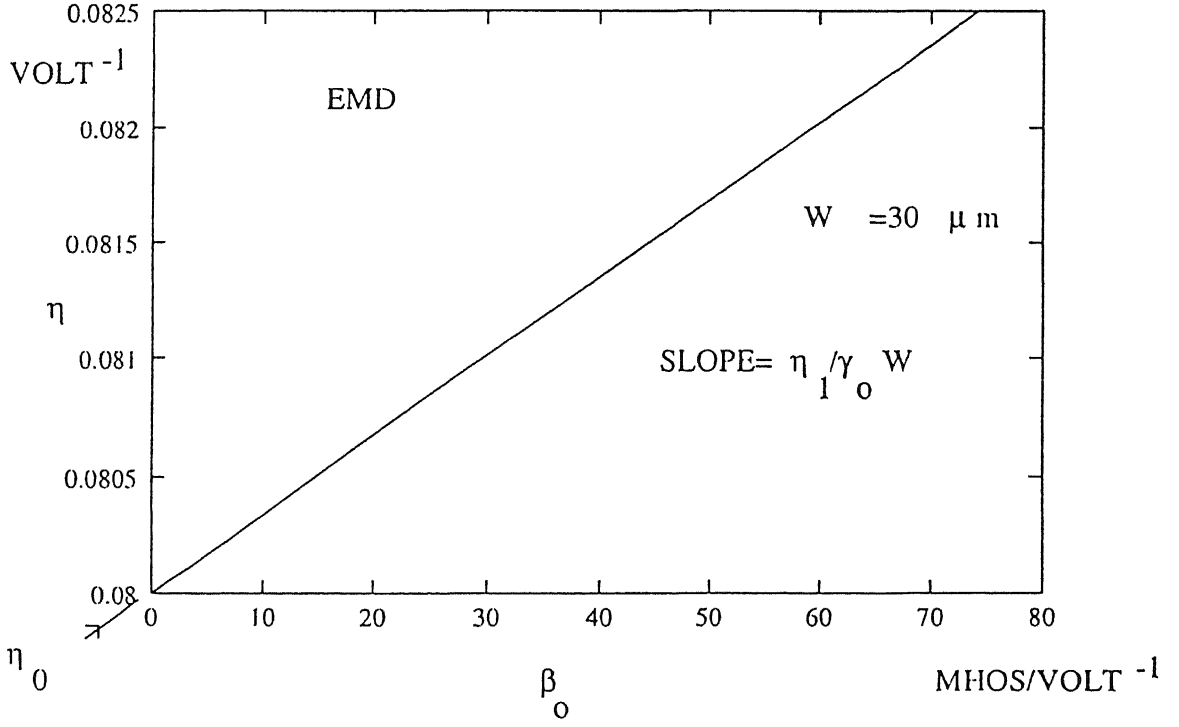


(b) Plot of $\frac{V_{ds}}{I_d}$ vs $[1/(V_{gs} - V_T - V_{ds}/2)]$ for constant

variable W



(a) Plot of $\frac{\theta}{\beta_o}$ vs $1/\beta_o$



(b)Plot of β_o vs η

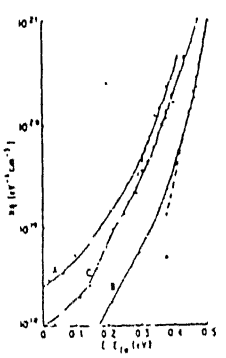
Figure 3.7: (a)-(b)

Chapter 4

The Model Of The Sub-Threshold Characteristics Of Poly-Si TFT

1 The Model

e electronic properties of a-Si and their relationship with deposition conditions are rela-
ly well characterized owing to the large amount of fundamental and applied work done
this material in past years. Models correlating TFT performance to the gap density of
es (DOS) have been formulated. Most of the characteristics work on this material has
n done for applications in integrated circuits such as a resistors and interconnections for
ch a detailed knowledge of the electronic properties of the material is not crucial. The
rmination of the density of states of poly-Si, based on the analysis of the transistor
acteristics. Density of states is continuous in energy and depends strongly upon the
morphology. Based on these, a new model for the characteristics of poly-Si TFTs is
ced. We assume here negligible free carrier concentration and small drain voltage V_D



13
FIG. 1. Density of states for three samples: (1) polysilicon thickness 0.6 μm (A); (2) polysilicon thickness 1.5 μm (B), (3) sample A after hydrogenation (C).

and the polysilicon film consists of 2-dimensional grain of length a. Poisson's equation near a grain boundary at y=0 as shown in fig.B.1 of Appendix B;

$$\frac{\partial^2\psi}{\partial x^2}+\frac{\partial^2\psi}{\partial y^2}=\frac{S(x)\delta(y)}{\epsilon_s} \tag{4.1}$$

where x is the direction perpendicular to the channel, ψ is the electrostatic potential , S(x) is the grain boundary charge per unit area, $\delta(y)$ is Dirac's $\delta-$ function and ϵ_s is the semiconductor dielectric constant. As for the boundary conditions for $V_D = 0$, symmetry considerations require:

$$\frac{\partial\psi}{\partial y}|_{\pm a/2}=0 \tag{4.2}$$

Thus, for small V_D it is reasonable to write:

$$\frac{\partial\psi}{\partial y}|_{\pm a/2}=\frac{V_D}{L} \tag{4.3}$$

TFT subthreshold characteristics i.e. $V_D \simeq 0$ or V_d is small. Where L is the channel length. By integrating Poisson's equation with these two conditions from $\frac{-a}{2}$ to $\frac{a}{2}$:

$$\frac{\partial^2\overline{\psi}}{\partial x^2}=\frac{e(x)}{\epsilon_s} \tag{4.4}$$

where

$$\overline{\psi}=\frac{1}{a}\int_{-a/2}^{a/2}\psi(x,y)dy \tag{4.5}$$

and e(x)=S(x)/a. When the Debye length L_D is much longer than the grain size, $\overline{\psi} = \psi(x,0) = \psi(x.+a/2)$ and the problem is reduced to a 1-dimensional one, where e(x) is the average charge density per unit volume. Since the polysilicon used for TFTs is either undoped or lightly doped, and a $\sim$ 100-1000Å. From eq(4.4)

$$2\frac{\partial\psi}{\partial x}\frac{\partial^2\psi}{\partial x^2}=2\frac{\partial\psi}{\partial x}\frac{e(x)}{\epsilon_s} \tag{4.6}$$

$$\frac{d}{dx}(\frac{d\psi}{dx})^2=2\frac{d\psi}{dx}\frac{e(x)}{\epsilon_s} \tag{4.7}$$

Integrating above eq.

$$\int_0^{x_0}\frac{d}{dx}(\frac{d\psi}{dx})^2dx=\int_0^{x_0}2\frac{d\psi}{dx}\frac{e(x)}{\epsilon_s}dx \tag{4.8}$$

$$(\frac{d\psi}{dx}|_{x=x_0})^2-(\frac{d\psi}{dx}|_{x=0})^2=\frac{2}{\epsilon_s}\int_{\psi_s}^{0}e(\psi)d\psi \tag{4.9}$$

$$(\frac{d\psi}{dx}|_{x=x_0})^2=\frac{2}{\epsilon_s}\int_{\psi_s}^{0}e(\psi)d\psi \tag{4.10}$$

In n-channel TFT, for the DOS in the upper half of the gap, it can be assumed without loss of generality, and consistent with the experimental data, taken from reference (7) and (8) of Bibliography:

$$N(E) = N_G exp((E - E_C)/KT_G) \tag{4.11}$$

where N_G is the density of the gap states immediately below the conduction band edge E_c and KT_G is the characteristics energy of the exponential band tail. By multiplying both sides of eq.(4.4) by $d\psi$ and integrating in x from the interface (x=0, $\psi = \psi_s$) to the back surface (x=d, $\psi = 0$) We get:

$$(\frac{d\psi}{dx})^2 = \frac{2}{\epsilon_s}\int_0^{\psi_s} e(\psi)d\psi \tag{4.12}$$

To approximate the Fermi function to a step function, which is reasonable for low enough temperatures.

$$(\frac{d\psi}{dx})^2 = F^2 L(\psi_s) \tag{4.13}$$

where:

$$L(\psi_s) = \exp(q\psi_s/KT_G) - q\psi_s/KT_G - 1 \tag{4.14}$$

$$F^2 = 2N_T KT_G/\epsilon_s \tag{4.15}$$

$$N_T = N_G KT_G \exp((E_F - E_C)/KT_G) \tag{4.16}$$

The channel sheet conductance (G) of the device is,

$$G = G_0 + G_0/d\int_0^d (\exp(q\psi(x)/KT) - 1)dx = G_0 + G_0/d\int_0^{\psi_s} \frac{\exp(q\psi/KT) - 1}{d\psi/dx}d\psi \tag{4.17}$$

where $G_0$is the flat band sheet conductance. We assume here for simplicity n-type conductivity in the flat band conditions:

$$G_0 = q\mu dN_c \exp((E_f - E_c)/KT) \tag{4.18}$$

Eq(4.17) by differentiation gives:

$$\frac{dG}{d\psi_s} = \frac{-G_0}{d}\frac{\exp(q\psi_s/KT) - 1}{(d\psi/dx)x = 0} \tag{4.19}$$

knowing,

$$V_G - V_{FB} = V_{0x} + \psi_s \tag{4.20}$$

From eq.$(\frac{d\psi}{dx})^2|_{x=0} = F^2 L(\psi_s)$ Assume,

$$(\frac{d\psi}{dx})^2|_{x=0} = F^2 exp(q\psi_s/kT_G) \tag{4.22}$$

$$\frac{dG}{d\psi_s} = -\frac{G_0}{d}\frac{exp(q\psi_s/kT)}{Fexp(\frac{q\psi_s}{2kT_G})} \tag{4.23}$$

$$\frac{dG}{d\psi_s} = -\frac{G_0}{dF}exp(q\psi_s/kT - \frac{q\psi_s}{2kT_G}) \tag{4.24}$$

$$\frac{dG}{d\psi_s} = -\frac{G_0}{dF}exp((q\psi_s/kT_G)(2\frac{T_G}{T} - 1)) \tag{4.25}$$

neglecting the effect of interface states,

$$V_G - V_{FB} = t_{ox}\frac{\epsilon_s}{\epsilon_{ox}}\frac{d\psi}{dx}|_{x=0} + \psi_s \tag{4.26}$$

For small ψ_s

$$V_G - V_{FB} \simeq t_{ox}\frac{\epsilon_s}{\epsilon_{ox}}\frac{d\psi}{dx}|_{x=0} \tag{4.27}$$

$$V_G - V_{FB} \simeq t_{ox}\frac{\epsilon_s}{\epsilon_{ox}}Fexp\frac{q\psi_s}{2kT_G} \tag{4.28}$$

$$exp\frac{q\psi_s}{2kT_G} = \frac{V_G - V_{FB}}{t_{ox}\frac{\epsilon_s}{\epsilon_o}F} = \frac{V_G - V_{FB}}{V_0} \tag{4.29}$$

using above equations we have

$$\frac{dG}{d\psi_s} = -G_0/dF(\frac{V_G - V_{FB}}{V_0})^{(\frac{2T_G}{T}-1)} \tag{4.30}$$

further

$$\frac{dV_G}{d\psi_s} = \frac{t_{ox}\epsilon_s Fq}{\epsilon_o 2kT_G}exp(\frac{q\psi_s}{2kT_G}) \tag{4.31}$$

$$\frac{dV_G}{d\psi_s} = \frac{t_{ox}\epsilon_s Fq}{\epsilon_o 2kT_G}(\frac{V_G - V_{FB}}{V_0}) \tag{4.32}$$

$$\frac{d\psi_s}{dV_G} = \frac{\epsilon_o 2kT_G}{t_{ox}\epsilon_s Fq}(\frac{V_0}{V_G - V_{FB}}) \tag{4.33}$$

$$\frac{dG}{dV_G} = \frac{dG}{d\psi_s}\frac{d\psi_s}{dV_G} \tag{4.34}$$

$$\frac{dG}{dV_G} = \frac{G_0\epsilon_{ox}2kT_G}{qdF^2\epsilon_s t_{ox}}(\frac{V_G - V_{FB}}{V_0})^{(\frac{2T_G}{T}-2)} \tag{4.35}$$

using

$$F^2 = 2N_T kT_G/\epsilon_s \tag{4.36}$$

$$\frac{dG}{dV_G} = \frac{G_0\epsilon_{ox}}{qN_T dt_{ox}}(\frac{V_G - V_{FB}}{V_0})^{(\frac{2T_G}{T}-2)} \tag{4.37}$$

Integrating

$$G - G_0 = \frac{G_0 \epsilon_{ox}}{qN_T dt_{ox}} \frac{1}{2T_G/T - 1} \frac{(V_G - V_{FB})^{2T_G/T-1}}{(V_0)^{2T_G/T-2}} \tag{4.38}$$

$$G - G_0 = \frac{G_0 \epsilon_{ox}}{qN_T dt_{ox}} \frac{T}{2T_G - T} \frac{(V_G - V_{FB})^{2T_G/T-1}}{(V_0)^{2T_G/T-2}} \tag{4.39}$$

$$F^2 = 2N_T \frac{KT_G}{\epsilon_s} \tag{4.40}$$

$$G_0 = q\mu d N_C exp((E_F - E_C)/kT) \tag{4.41}$$

$$N_T = N_G kT_G exp((E_F - E_C)/kT_G) \tag{4.42}$$

$$V_0 = \frac{\epsilon_s t_{ox}}{\epsilon_{ox}} (\frac{2N_T kT_G}{\epsilon_s})^{1/2} \tag{4.43}$$

$$V_0{}^{2\frac{T_G}{T}-2} = (\frac{\epsilon_s t_{ox}}{\epsilon_{ox}})^{2\frac{T_G}{T}-2} (\frac{2N_T kT_G}{\epsilon_s})^{\frac{T_G}{T}-1} \tag{4.44}$$

$$\frac{G_0}{N_T} = \frac{q\mu d N_C}{N_G kT_G} exp[\frac{E_F - E_C}{kT} - \frac{E_F - E_C}{kT_G}] \tag{4.45}$$

$$\frac{G_0}{N_T} = \frac{q\mu d N_C}{N_G kT_G} exp[\frac{E_F - E_C}{kT_G}(\frac{T_G}{T} - 1)] \tag{4.46}$$

$$\frac{G_0}{N_T} = \frac{q\mu d N_C}{N_G kT_G} (\frac{N_T}{N_G kT_G})^{\frac{T_G}{T}-1} \tag{4.47}$$

$$K_0 = \frac{G_0 \epsilon_{ox}}{qN_T dt_{ox}} (\frac{T}{2T_G - T})(\frac{1}{V_0})^{\frac{2T_G}{T}-2} \tag{4.48}$$

$$K_0 = \frac{\epsilon_{ox} N_T q\mu d N_C}{qdt_{ox} N_G kT_G} (\frac{N_T}{N_G kT_G})^{\frac{T_G}{T}-1} \frac{T}{2T_G - T} (\frac{\epsilon_{ox}}{\epsilon_s t_{ox}})^{\frac{2T_G}{T}-2} (\frac{\epsilon_s}{N_T})^{\frac{T_G}{T}-1} (\frac{1}{2kT_G})^{\frac{T_G}{T}-1} \tag{4.49}$$

$$K_0 = q\mu N_C (\frac{T}{2T_G - T})(\frac{2\epsilon_s}{N_G q^2})^{1/2} (\frac{\epsilon_{ox}{}^2}{2\epsilon_s t_{ox}{}^2 k^2 T_G{}^2 N_G})^{(\frac{T_G}{T}-\frac{1}{2})} \tag{4.50}$$

where

$$V_0 = \epsilon_s t_{ox} F/\epsilon_{ox} \tag{4.51}$$

It is above derived that the integration of eq.(4.37) gives:

$$G - G_0 = K_0(V_G - V_{FB})^{(2T_G/T-1)} \tag{4.52}$$

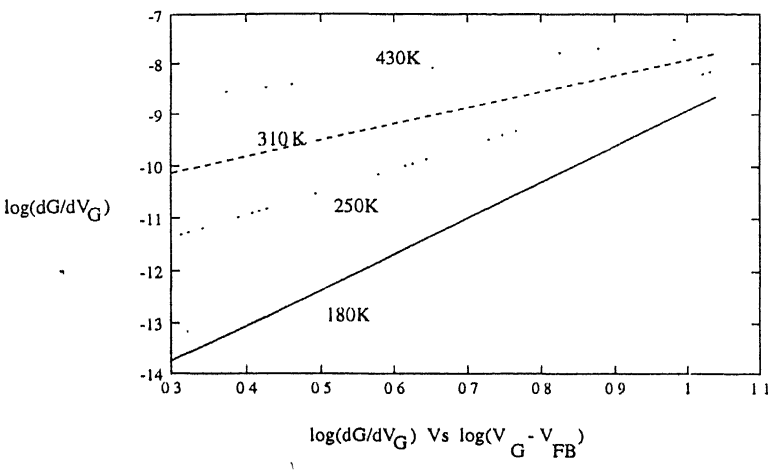
where $K_0 = q\mu N_c(T/(2T_G - T))(2\epsilon_s/N_G q^2)^{1/2}(\epsilon_{ox}{}^2/(2\epsilon_s t_{ox}{}^2 N_G K^2 T_G{}^2))^{(T_G/T-1/2)}$ (The programme for Sub Threshold characteristics of TFT is presented in sec C 2 of Appendix C.)

4.2 Results

The subthreshold characteristics of polysilicon TFTs are explained by neglecting the discrete grain structure and assuming a spatially distributed concentration of defects. The mathematical modelling of the dG/dV_G vs $V_G - V_{FB}$ equations presented here is more direct and gives a better idea of the approximations involved. At different temperatures, plots gives the validity of the approach.

A plot of $\log(\frac{dG}{dV})$ vs $\log(V_G - V_{FB})$ should give a straight line of slope $2\frac{T_G}{T} - 2$ and the characteristics parameter of the exponential band tail T_G can be determined. This is shown in fig.4.1.

A plot of LOG(G) vs V_G is shown in fig.4.2 which gives G-V_G characteristics for T=310 K.



$N_c = 1.3 \times 10^{25}\ m^{-3}$

$N_G = 3 \times 10^{26}\ m^{-3} eV^{-1}$

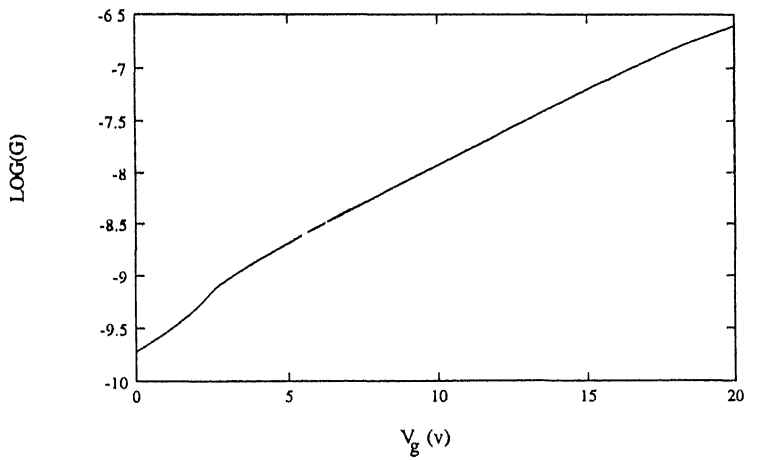
$E_c - E_F = .42\ meV$

$\mu = 5\ cm^2/Vs$

$\frac{KT_G}{q} = 69\ mV$

$T_G = 800K$

Figure 4.1:



$N_c = 3.2 \times 10^{25}\ m^{-3}$

$N_G = 3 \times 10^{26}\ m^{-3} eV^{-1}$

$E_c - E_F = .42\ eV$

$\mu = 5\ cm^2/Vs$

$\frac{KT_G}{q} = 69\ mV$

$T_G = 800K$

3.2 A theoretical G-v_G characteristics for T=310 K.

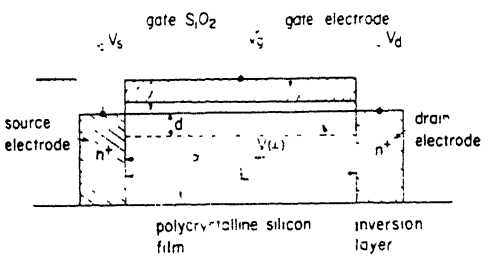
Figure 4.2:

Chapter 5

Modelling for accumulation mode of Poly-Si TFT

5.1 The Model

A schematic of polysilicon TFT is shown in fig.(5.I).
Polysilicon thin film transistor consists of polysilicon film usually grown by low-power chemical vapour deposition (LPCVD) approximately 1000Åthick Gate oxide (1000Å) and polysilicon gate electrode (3000Å) is deposited on the polysilicon film. The source and drain are formed by doping using ion-implatation and subsequent annealing. Polysilicon TFT is driven



Cross section of polycrystalline thin-film transistor showing the symbols used in the text

[10]

fig.(5.I)

into accumulation mode when gate voltage V_g ,exceeding the threshold voltage V_{th} is applied to the poly-Si TFT. The carriers, which are electrons in the n-channel mode, are induced near the polysilicon film surface, and a strong inversion layer is formed. The carrier concen-

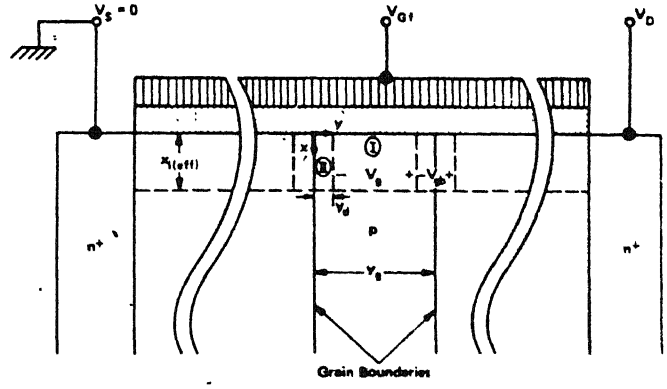
tration n(x) in the strong-inversion layer for potential V(x) at the distance x from the source electrode is

$$n(x) = C_{ox}(V_g - V_{th} - V(x))/q.d \tag{5.1}$$

where C_{ox} is gate oxide capacitance, and q and d are the electronic charge and inversion layer thickness, respectively. For strong inversion conditions within the grains, electron trapping at localized grain-boundary states produces potential barriers that effect the electron transport along the channel. The barrier formation is similar to that at grain boundaries in bulk polysilicon, except in the channel $\psi(x)$ is influnced by V_g as described by the two dimensional form of poisson's equation.

Consider the potential variation near a grain boundary in the channel as shown below.

It is assumed that away from the grain boundary (y > y_d) the electric field is vertical (in



Cross section of effective inversion layer showing typical grain and grain boundaries, which are assumed to be perpendicular to the electron flow.

Figure 5II [19]

the x-direction), and the true electron distribution n(x) is well approximated by n(x) over the effective inversion layer, $0 \leq x \leq x_{i(eff)}$. In this region poisson's equation simplifies to

$$(\frac{\partial^2\psi}{\partial x^2})|_I \simeq \frac{q}{\epsilon_s}(n(x) + N_A) \tag{5.2}$$

where ψ is electrostatic potential. It is assumed that that trapping nearly depletes the region (II) of free electrons;hence

$$(\frac{\partial^2\psi}{\partial x^2})|_{II} + (\frac{\partial^2\psi}{\partial y^2})|_{II} \simeq \frac{q}{\epsilon_s}(N_A) \tag{5.3}$$

Assuming that, analogus to the gradual channel approximation, the trapped electrons at the grain boundary typically create only a small perturbation on the x-component of electric field, so

$$|(\frac{\partial^2\psi}{\partial x^2})|_I - (\frac{\partial^2\psi}{\partial x^2})|_{II} << |(\frac{\partial^2\psi}{\partial y^2})|_{II}| \tag{5.4}$$

where partial derivatives are evaluated anywhere in the regions indicated. From the comination of (5.2)-(5.4), the corresponding approximation for $\psi(x)$

$$(\frac{\partial^2\psi}{\partial x^2})|_{II} \simeq (-\frac{q}{\epsilon_s})n(x) \tag{5.5}$$

with the boundary conditions

$$\psi(x, y = y_d) = \psi_I(x) \tag{5.6}$$

and

$$\frac{\partial\psi}{\partial y}|_{y=y_d} = 0 \tag{5.7}$$

The solution to (5.5)-(5.7) is

$$\psi(x, y)|_{II} \simeq \frac{-qn(x)}{2\epsilon_s}(y - y_d)^2 + \psi_I(x) \tag{5.8}$$

and hence grain boundary potential

$$\psi(x) = \psi_I(x) - \psi(x, 0)|_{II} \simeq \frac{qn(x){y_d}^2}{2\epsilon_s} \tag{5.9}$$

By the conservation of charge in the vicinity of the grain boundary

$$Q_{GB} = -2qn(x)y_d \tag{5.10}$$

The trapped charge density depends on the distribution in the energy gap of localized grain boundary states. By approximating this distribution by a delta function yielding N_{st} states (traps) per unit area at energy levels E_F. Then eq (5.11)

$$Q_{GB} = \frac{-qN_{st}}{1 + \frac{1}{2}exp\{\frac{[E_T - E_F]_{y=0}}{kT}\}} \tag{5.11}$$

where E_F is the fermi level and factor $1/2$ reflects the degeneracy of the localized states. The position of E_F relative to E_T is defined by $\psi(x)$ and the electron density in region I, n(x)

$$[E_T - E_F]_{y=0} \simeq [E_T - E_i] + q\psi(x) - kTln(\frac{n(x)}{n_i}) \tag{5.12}$$

where E_i is the intrinsic Fermi level and n_i is the intrinsic carrier density in silicon. V_g is sufficiently high, $\psi(x)$ decreases with increasing V_g, and hence $Q_{GB} \simeq -qN_{st}$ is independent of V_g. From eq (5.9) and (5.10)

$$\psi(x) \simeq \frac{qN_{st}{}^2}{8\epsilon_s n(x)} \tag{5.13}$$

ıe induced carrier are trapped by trap levels at the grain boundary, which form a potential rrier. When the gate voltage is high, all carrier trap levels are filled. The expression for rrier potential height

$$\psi(x) = qN_{st}{}^2/8\epsilon n(x) \tag{5.14}$$

In the other case, at low gate voltage, the carrier ıp levels at the grain boundary are not completely filled due to the low carrier concentration luced by the gate voltage. Therefore Fermi level is near the position of the carrier trap vel. The potential barrier height $\psi(x)$ is approximated over a wide range of gate voltage

$$\psi(x)^{-1} = \psi_0{}^{-1} + (qN_{st}{}^{-1}/8\epsilon n(x))^{-1} \tag{5.15}$$

ıis results in a virtual fixing of the potential barrier at ψ_0 which is ~ 0.55V corresponding half the energy gap of silicon. Assuming that the carrier concentration taking part in e conductivity is not the total grain-carrier concentration n(x), but an activated carrier ncentration n(x)' defined by.

$$n(x)' = n(x)\exp(-q\psi(x)/kT). \tag{5.16}$$

r the interpretation of the hall effect it was assumed that the carrier concentration taking rt in the conductivity is the total grain carrier concentration n(x) and the mobility is tivated and has the form $\mu = \mu_0 e^{-q\psi(x)/kT}$.

hen the mean free path in the grain is short compared to the grain size, account should be ken of the scattering in the grain. In the general case the total resistivity ρ has contributions ım both the grains ρ_G and their boundaries ρ_B. Then it is written,

$$\rho = \rho_G + \rho_B = \frac{1}{q\mu_G n_0} + \frac{1}{q\mu_b n_0 exp(-q\psi(x)/kT)} \tag{5.17}$$

ıere μ_G is the grain mobility. Now, it can be written as $\mu(x)^{-1} = \mu_g{}^{-1} + (\mu_b \exp(-q\psi(x)/kT))^{-1}$ ırrier scattering takes place at the grain boundary to a greater extent. Then in the grain, obility μ_b at the grain boundary is less than the grain mobility μ_g in good quality grains.

$$\begin{aligned}\mu(x)^{-1} &= \mu_g{}^{-1} + (\mu_b \exp(-q\psi(x)/kT))^{-1} \\ &\simeq (\mu_b exp(-q\psi(x)/kT))^{-1}\end{aligned} \tag{5.18}$$

ıe gradual channel approach gives the current-voltage relations for poly-Si TFT's with the annel length L and width W in the region of $(V_g - V_{th}) > V_d$

$$I = (W/L)C_{ox}\int_0^{V_d} \mu_b(V_g - V_{th} - V(x)).\exp(-q\psi(x)/kT)dV(x) \tag{5.19}$$

where V_d is the drain voltage. For the region of $V_g - V_{th} >> V_d$, the current voltage characteristics is defined as

$$I = (W/L)C_{ox}\mu^*((V_g - Vth)V_d - {V_d}^2/2) \tag{5.20}$$

where μ^* is effective mobility and this is given

$$\mu^* = \mu_b \exp(-q\psi'/kT) \tag{5.21}$$

ψ' indicates the effective potential barrier height in the region and is given by

$$\psi' = \alpha/(V_g - V_{th} + \alpha/\psi_0) \tag{5.22}$$

$$\alpha = q^2{N_{st}}^2 d/8\epsilon C_{ox} \tag{5.23}$$

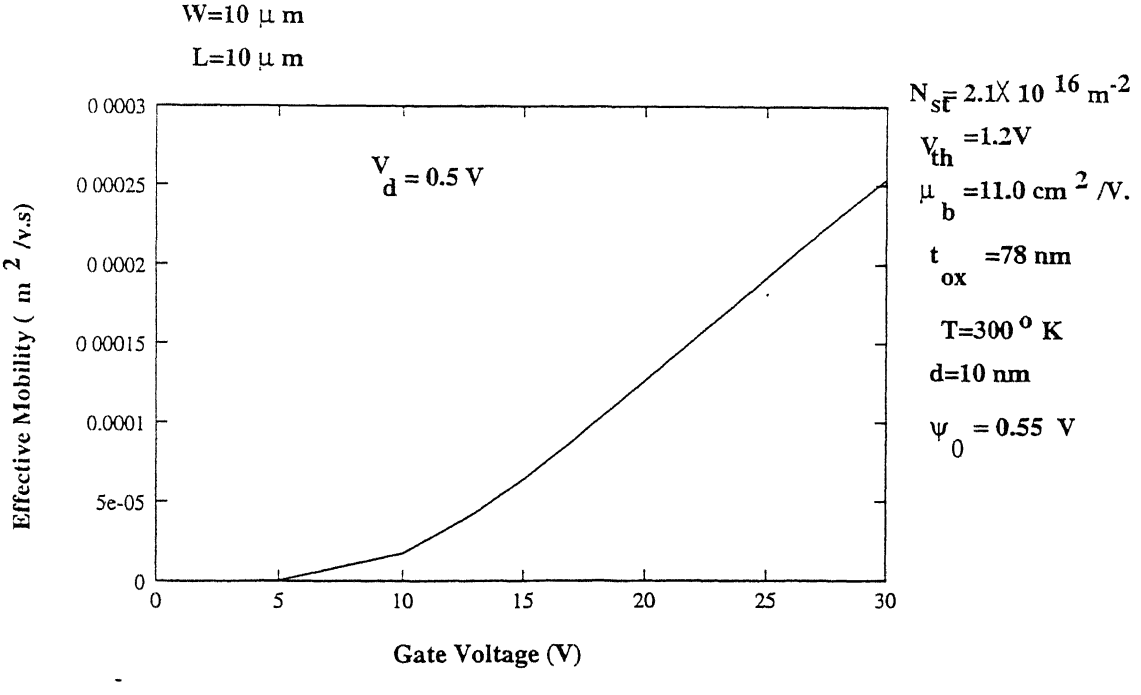
(The programme for accumulation mode of TFT is presented in sec.C.1 of Appendix C.)

5.2 Results

Fig.5.1 shows changes of effective mobility as a function of gate voltage using equation(5.21). The effective mobility increases with an increase in the gate voltage.

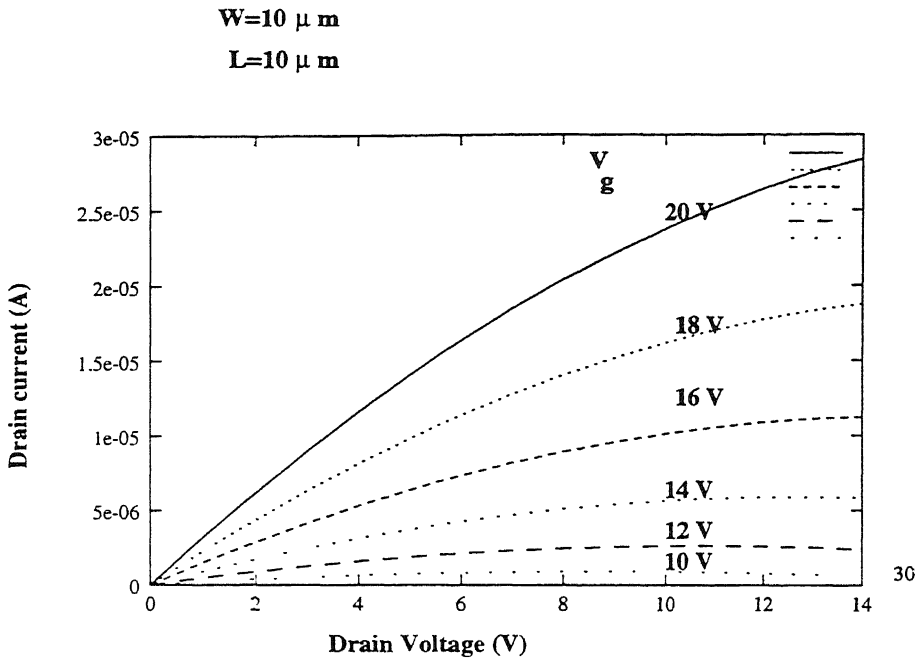
The I-V characteristics were calculated using equation 5.21 for different gate voltage. Fig.5.2 shows I-V charcteristics of polycrystalline silicon TFT .

Fig.5.3 shows changes of potential barrier height as a function of gate voltage using equation 5.22. These all figures showa good agreement with experiment data (taken from reference (10)).



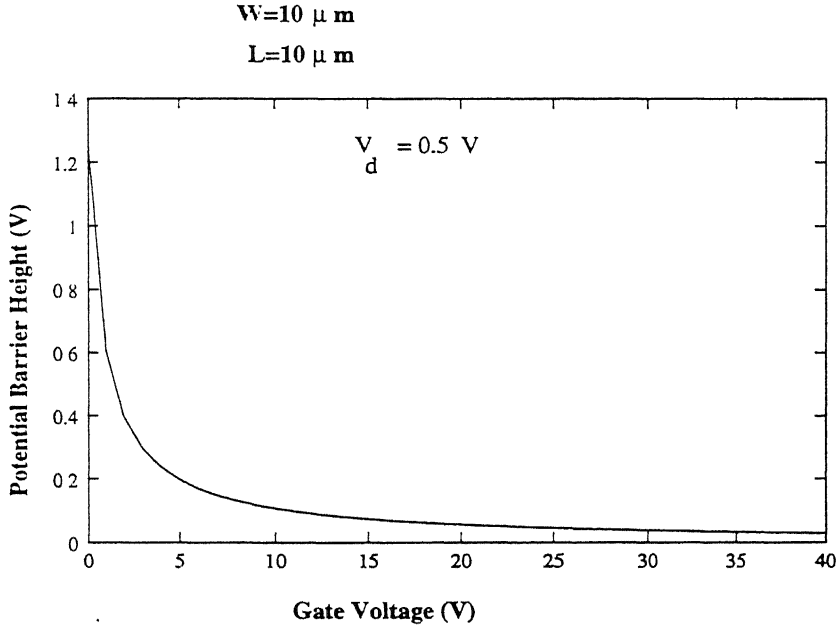
5.1 Effective mobility vs gste voltage

Figure 5.1:



5.2 Plot of I_d vs V_d at different V_g .

Figure 5.2:



5.3 Plot of potential barrier height vs gate voltage

Figure 5.3:

Chapter 6

Conclusion

The present work shows that the accuracy of the simple MOSFET current model can be significantly improved by including the effects of the entire bulk doping term, the dependence of carrier mobility on gate voltage, drain voltage, intrinsic resistance and channel length modulation.

The MOSFET model presented here describes the drain current-voltage characteristics of surface channel enhancement mode devices in strong inversion and ion-implanted depletion mode buried channel devices. This model also presents a method of extracting model parameters. In this MOSFET model, there is not included subthreshold conduction (soft turn on region) for depletion mode devices.

In this thesis, the TFT model presented here explains the subthreshold characteristics and accumulation mode of polycrystalline silicon thin film transistors by neglecting the discrete grain structure and assuming a spatially distributed concentration of defects. To account for the observed $I_D - V_G$ behaviour, it is essential that the density of states be continuous in energy. There is good fit of data with a DOS decreasing exponentially from the band edge towards the gap centre and with characteristics parameters, where expressions for G versus V_G is deduced . The mathematical derivation of the $\frac{dG}{dV_G}$ versus $V_G - V_{FB}$ equations is presented, here. That gives a better idea of the approximations involved. The mobility at the grain boundary and the carrier trap density could be easily obtained, the mobility and trap density exert a strong influence on polysilicon thin film transistors characteristics. In addition, it is found from calculations that the effective mobility increases with increase in gate voltage.

The following conclusions can be derived from present study:

the characteristics of the T.F.T. is similiar to that of the conventional FET, in so far as changes in the channel conductivity as a function of gate potential are concerned.

Appendix A

The analysis of MOSFET theory is divided into two sections: the first section gives a qualitative description of the workings of the MOS; the second section concentrates on a quantitative discussion which includes derivation derives the charactristic equations describing the MOS. The approximations made are used described below:

1. Mobility of current carriers in the channel is constant.
2. The variation of the channel thickness is small along the length of the channel.
3. The thickness of the dielectric over the channel region is assumed to be much greater than the channel thickness.
4. Parasitic resistances (such as in the source) are assumed to be so small as to be negligible.
5. The channel is completely shielded from the drain, so no drain-to-channel feedback exists.
6. Doping of the substrate is uniform and nondegenerate.
7. The drain current consists only of channel current. Leakage currents are neglected.
8. The gate dielectric is considered to be a perfect insulator.
9. Extrinsic conditions which affect the conduction properties-such as oxide traps, silicon surface states, interface energy states, ionic centers within the oxide, and work function differences will be lumped together into a single effective charge term, Q_{ss}. Furthermore, Q_{ss} is assumed to be constant and located at the silicon-oxide interface.

A.1 Short Channel Effects

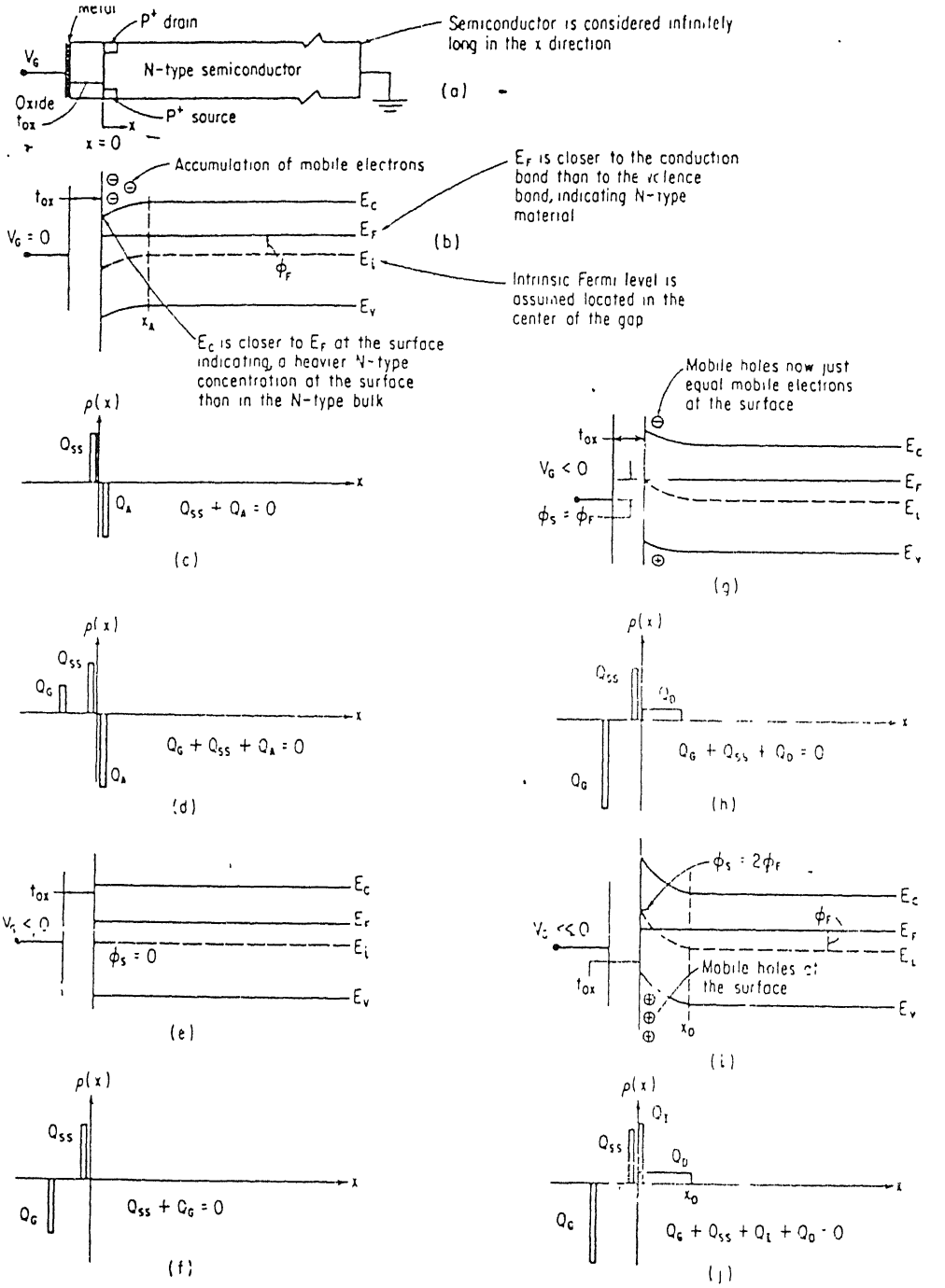
As the channel length is reduced, departure from long-channel behaviour, may occur. These departures, the short channel effects, arise as a result of a two dimensinol potential distribution and high electric fields in the channel region. When the channel length is reduced, the

tion and high electric fields in the channel region. When the channel length is reduced, the depletion layer widths of the source and drain junctions become comparable to the channel length. On account of this, potential distribution becomes two dimensional because it depends upon two fields transverse and longitudinal fields. This results in degradation of the subthreshold behaviour, dependence of the threshold voltage on the channel length and biasing voltages, and failure of current saturation due to punch through. The channel mobility is a function of field due to increase of electric field. When electric field is much higher than carrier multiplication near the drain occurs. High field also cause hot-carrier injection into the oxide.

A.2 Qualitative Analysis

Even though the following analysis refers specifically to a P-channel MOS on an N-type substrate (for convenience), the resulting equations are applicable to both N-channel and P-channel devices. There are three distinct conditions or regions occuring within the semiconductor at the surface, that are important to MOS operation. They are accumulation, depletion, and inversion regions and are controlled by the external bias on the gate electrode. Generally, for an oxide passivated surface, surface states or energy states at the silicon-oxide interface act as ionized doners whose effect is the same as a positive applied gate voltage. Figure A.1 shows the MOS structure used in this discussion. Drain-to-source voltage is assumed to be so small as to be negligible. The energy band diagram of a P-channel device under zero applied voltage is shown in figure. Here and in the following band-diagram , the intrinsic level ($P = N = n_i$) is designated as E_i and is assumed to be halfway between the conduction band energy E_c and the valence-band energy E_v. Because of the positive surface-state charge, negative electrons from within the N-type bulk are attracted to and accumulate at the surface (x=0). Accumulation results in a downward bending of the conduction and valence bands.

The closer E_c is bent toward the Fermi level, which is set by the substrate doping , the heavier the surface concentration of electrons becomes.Figure illustrates the charge density distribution. The positive charge per unit surface area (Q_{ss}) must be balancd by the negative charge accumulated near The silicon surface(Q_A). (Charge distributions are approximated by the delta functions) If a small positive bias is now applied to the gate, additional band



Energy-band and charge-distribution diagrams describing MOS operation: (*a*) Structure of the device used in this figure. (*b*) Energy-band diagram for the accumulation condition due to surface states. (*c*) Charge-density distribution due to surface states. (*d*) Charge-density distribution due to surface states in addition to positive applied gate voltage. (*e*) Energy-band diagram for the flat-band case. (*f*) Charge-density distribution for the flat-band case. (*g*) Energy-band diagram for the depletion case. (*h*) Charge-density distribution for the depletion case. (*i*) Energy-band diagram for the inversion case. (*j*) Charge-density distribution for the inversion case.

Figure A.1:

bending and accumulation result. Again, the total positive charge must equal the total negative charge so as to maintain charge neutrality ($Q_g + Q_{SS} + Q_A = 0$) . If a negative voltage is applied to the gate such that it just counters the effect of Q_{SS}, then no bending of the bands exists, a condition which is known as the flat band case ($\phi_S = 0$). Further application of negative gate voltage repels from the channel region the mobile electrons associated with donar centers, causing a depletion region to form. The band diagram and charge picture for this case are shown in figure. When electron is removed from its donar atom is left with a net positive charge. Thus the charge in the depletion region is shown as a positive charge, Q_D. in figure. When the intrinsic Fermi level E_i is bent just enough to intersect the Fermi level at x=0, the surface has gone from its initial N-type concentration to intrinsic (where P=N). (ϕ_s is now equal to ϕ_f.) Additional negative gate bias does not extend the depletion region so much as itinduces positive mobie holes at the surface. It is important to note that depletion region charge and mobile surface (channel) charge of the same polarity (positive) and thus their effects add. The sum of these two charge regions must balance the net charge stored in the oxide (Q_{SS}) and on the gate (Q_G) so as to maintain an electrically neutral system. As the gate bias is increased in the negative direction, a larger and larger percentage of the charge within the semiconductor is contributed by the mobile holes. Until $E_i = E_f$, mobile electrons still outnumber mobile holes. Beyond this point , electrons are suppressed below the intrinsic level while holes in the channel region raised above this level. As will be seen later, conduction between the P-type source and drain (by P-type carriers) does not become significant until holes dominate and provide the conducting path. One can level the onset of conduction (or the apparent onset of conduction, as will be discussed later;) as the threshold voltage V_{th} and define it as where the surface potential goes through intrinsic to a value of $\phi_s = 2\phi_f$. The threshold voltage is thus the gate voltage that produces a gate charge which just counterbalance the charge contained in surface states and in a depletion region that supports a voltage of $2\phi_f$. Further increases in gate voltage past V_{th} result in an increase in the number of holes, thus enhancing conduction between the source and drain.
It must be kept in mind that the start of actual conduction is not an abrupt process, in which channel is completely depleted of carriers at a given gate voltage V_G and then immediately acquires a finite inversion layer at a small increase in the magnitude of V_G. The minority and majority carriers within the channel are increasing and decreasing continuously and at a finite rate for changes in the gate voltage. Goldberg described the situation very nicely when he said "The transition from depletion to inversion is a continuous process, and one

must be aware of the fact that the minority carrier concentration increases as the majority carrier concentration decreases and that carriers are always present."

Examination of the gate capacitance as a function of the gate voltage can yield additional insight into the physical operation of the MOS. Starting with the accumulation condition, figure A.2 shows that the metal gate and the accumulation layer at the silicon surface firm a simple parallel-plate capacitor with a separation distance of t_{ox} and a normalized value of $C/C_o = 1$. Capacitance is measured at the gate, with the source, drain, and substrate grounded. As negative bias is applied, the depletion region that forms tends to separate the two plates of the capacitor and reduces the capacitance. (The two plates are now the gate electrode and the bulk silicon at the edge of the depletion region. Separation is $t_{ox} + x_D$). Further application of a negative gate bias attracts holes to the surface (inversion), which in effect decreases the distance seperating the two plates, thus increasing capacitance.

A.3 Quantitative Analysis

1. Linear Region. figure A.3 shows an idealized device together with the coordinate system that is used in the analysis. A brief outline of the "plan of attack" used to derive the device equations is as follows:

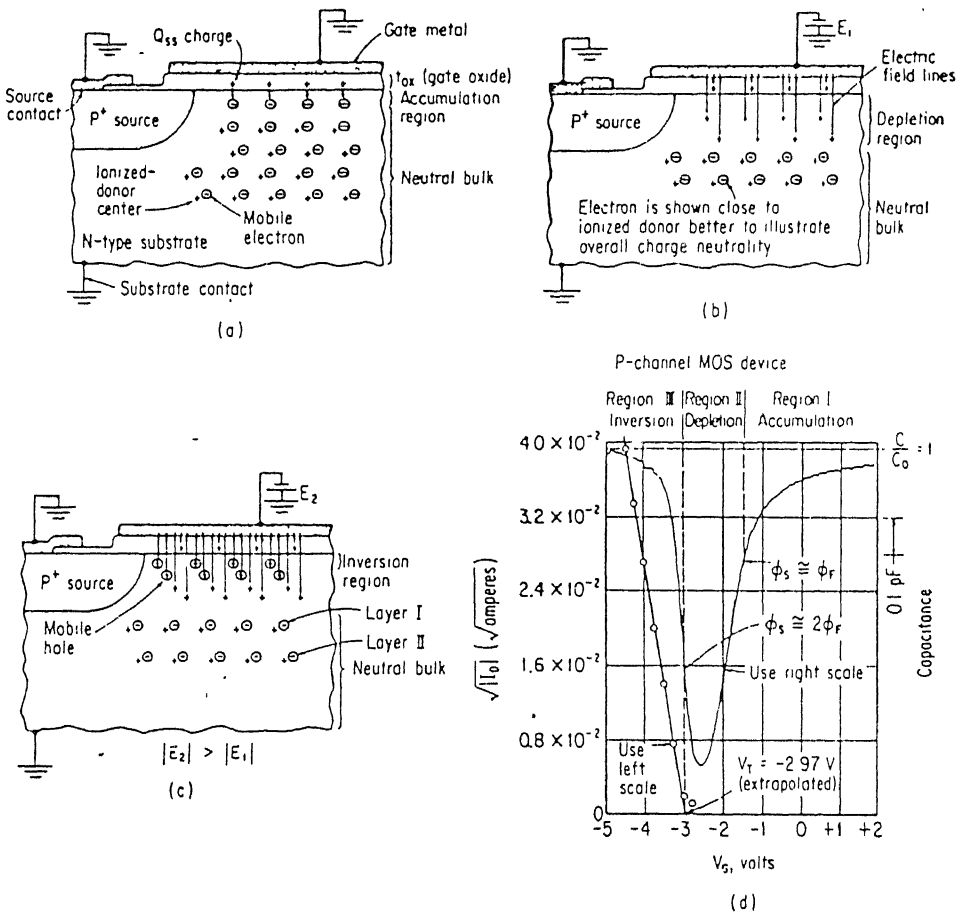
1. The channel-current density is integrated over a cross section of the channel (W dx) to obtain the current.
2. Channel current now a function of the charge in the channel.
3. This charge is found by summing all the system charge to zero.
4. Charge is now related to the gate voltage by the use of Gauss'law.
5. The expression for channel current can now be integrated over the length L of the channel.
6. Channel current can now be equated to the external terminal current.

Channel current can be written as

$$I_C = W \int J_c(x, y)dx \tag{A.1}$$

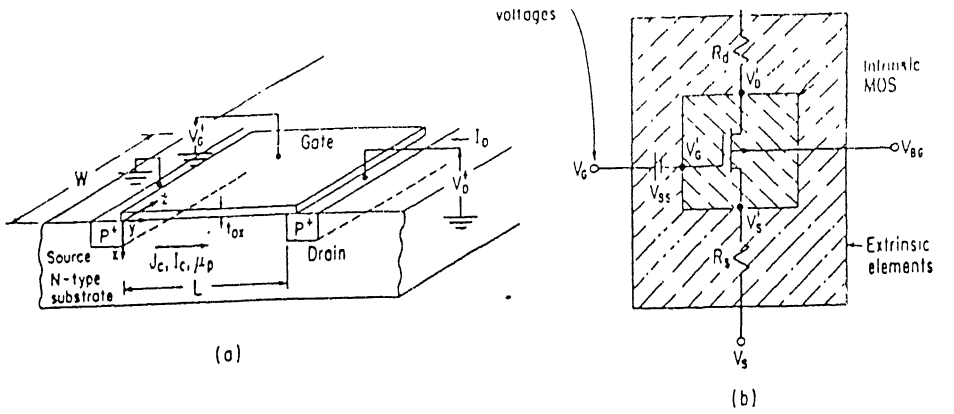
Where W indicates channel width in the z direction. W is perpendicular to the direction of current flow.

From Ohm's law,



Diagrams illustrating the position of charge under the gate as a function of bias: (*a*) accumulation case; (*b*) depletion case; (*c*) inversion case; (*d*) C vs V_G plot of MOS gate showing the three characteristic regions together with a plot of $\sqrt{|I_D|}$ vs. V_G.

Figure A.2:



(a) Diagrammatic sketch of an MOS showing dimensions and directions used for analysis.
(b) Diagram illustrating the intrinsic and extrinsic elements of an MOS.

Figure A.3:

$$J_c(x,y) = \nu(x)E_y = q\mu_p P(x)E_y \tag{A.2}$$

) that

$$I_C = W\int q\mu_P E_y P(x)dx \tag{A.3}$$

',

$$I_C = Wq\mu_p E_y \int p(x)dx \tag{A.4}$$

ι_p is constant and independent of x . μ_p is a positive number, while μ_n is negative.]
ow E_y = -($\frac{dV}{dy}$), so that

$$-I_C = W\mu_p \frac{dV}{dy} q\int p(x)dx \tag{A.5}$$

Where$q\int p(x)dx$ represents the mobile charge per unit area in the channel. The problem now reduced to evaluating $q\int p(x)dx$. Since the total MOS-system charge must equal zero

$$Q_G + Q_{SS} + Q_C + Q_D = 0 \tag{A.6}$$

Where
$_G+Q_{SS}$ represents all the charge outside of the semiconductor material proper and Q_C+Q_D presents all the charge within the semiconductor material . The channel charge is thus

$$-Q_C = Q_G + Q_{SS} + Q_D \tag{A.7}$$

The charge induced by the gate can be related to the gate voltage by Gauss's law , which states

$$\int E_{ox}(S)dS = \frac{Q_{total}}{\epsilon_{ox}} \tag{A.8}$$

$$\epsilon_{ox}E_{ox}W\,dy = Q_{total} \tag{A.9}$$

E_{ox} is defined as
$-\frac{dV_{ox}}{dx}$
where dV_{ox} = voltage across the oxide
dx= oxide thickness now

$$-\frac{dV_{ox}}{dx} = -\frac{\Delta V_{ox}}{\Delta x} \tag{A.10}$$

Where

$$\Delta x = +t_{ox} \tag{A.11}$$

$$\Delta V_{ox} = -[V_G - V(y)] \tag{A.12}$$

so that

$$-\frac{dV_{ox}}{dx} = +\frac{V_G - V(y)}{t_{ox}} \tag{A.13}$$

(The voltage across the oxide is simply the gate voltage minus the voltage on the channel. channel voltage will be a function of the distance in the y direction, ranging from V_D at the drain to zero volts at the source.) Inserting Equation A.7 into Equation A.13 and letting $\frac{\epsilon_{ox}}{t_{ox}} = C$(capacitance per unit area)yield

$$Q_G = [V_G - V(y)]C \tag{A.14}$$

Equation A.14 relates the product of the gate capacitance per unit area and the voltage across the oxide to the charge per unit area under the gate. The gate charge found :

$$Q_C = -[V_G - V(y)]C - (Q_{SS} + Q_D) \tag{A.15}$$

Equation (A.13) is a mathematical statement of the amount of mobile charge contained in the channel per unit area. Keep in mind that this is the charge that allows conduction between the source and drain. Q_C will be enhanced by the gate voltage V_G, decreased by the channel voltage created by the drain supply, V(y) , decreased by the charge stored in the depletion region beneath the channel, Q_D, and either increased or decreased by Q_{SS}, depending upon its polarity. Later it will be interesting to investigate the condition required

the cause the channel charge to go to zero.

Note that $Q_C = q\int p(x)dx$, which is the desired quantity of Eq.(A.5). Substituting Eq.(A.5) into Eq.(A.13) yields

$$-I_C = W\mu_p \frac{dV}{dy} - [V_G - V(y)]C - (Q_{SS} + Q_D) \tag{A.16}$$

Factoring out C,

$$I_C dy = W\mu_p C dV\{\left[V_G - V(y)\right] + \frac{Q_{SS} + Q_D}{C}\} \tag{A.17}$$

Equation A.17 can now be integrated between 0 and L for the length and between 0 and V_D for the voltage:

$$I_C \int dy = W\mu_p C[V_G \int_0^{V_D} dV - \int V(y)dy + \frac{Q_{SS} + Q_D}{C} \int dV] \tag{A.18}$$

$$I_C L = W\mu_p C(V_G V_D - 1/2V_D^2 + \frac{Q_{SS} + Q_D}{C} V_D) \tag{A.19}$$

Now

$$C = C_o/WL \tag{A.20}$$

and

$$I_C = -\frac{C_O \mu_p}{L^2}[-V_G - V_{th})V_D + 1/2V_D^2] \tag{A.21}$$

where

$$V_{th} = -(Q_{SS} + Q_D)/C. \tag{A.22}$$

(the threshold-voltage term will be discussed in more detail in

Equation A.21 can also be written as

$$I_C = -\beta[-(V_G - V_{th})V_D + 1/2V_D^2] \tag{A.23}$$

$$\beta = \frac{W\epsilon_{ox}\mu_p}{Lt_{ox}} \tag{A.24}$$

Where (Because of the sign convention for μ, β_p is positive and β_n is negative.) Now the channel current of the Equation $I_C + I_D = 0 or I_C = -I_D$. The final form of the equation for the drain current of a device in the triode region can be written as

$$I_D = -\beta[(V_G - V_{th})V_D - 1/2V_D^2] \tag{A.25}$$

This equation A.25 assumes no drain or source resistance . At this point, it is easy to include the effects of a given parasitic resistance R_d and R_s. Equation A.17 is integrated from 0 to L on the left hand side and from V_S' to V_D' on the right hand side. This integration yields

$$I_D = \beta[(V_G - V_{th})(V_D' - V_S') - 1/2(V_D'^2 - V_S'^2)] \tag{A.26}$$

Which represents the triode region drain current.

$$V_D' = V_D - I_D R_D \tag{A.27}$$

$$V's = I_S R_s \tag{A.28}$$

The saturation drain current can be written as

$$I_D = -\beta \frac{(V_G - V_p)^2}{1 - \beta R_d(V_G - V_p) + \sqrt{(1 - 2\beta R_d(V_G - V_p))}} \tag{A.29}$$

Equation A.29 was used to generate the triode portion of the charactristic curves for P-channel device .

The output current in the triode region depends upon the drain voltage, and hence the drain source terminals are like a resistor whose value depends upon the gate bias. Using a small signal approximation, the resistance is linear and adjustable. Close to the origin and when $|V_D| << |V_G - V_{th}|$, the resistive characteristics are quite linear over a range of voltages and currents. Since the curves pass through the origin, the characteristics suggest that the MOS can be used as a voltage controlled d-c, as well as a-c, resistor. Equation was derived on the basis of the gradual channel approximation and is valid only for the case where $|V_D| << |V_G - V_{th}|$. When $|V_D| >= |V_G - V_p|$, the device enters the saturation or

pinch off region . Equation A.29 is not also valid in the low current region when $V_G = V_{th}$. Here the inversion layer is not yet fully formed, and the gate electric field terminates on comparable quantities of mobile charge (in the channel area) and immobile charge (in the depletion region beneath the channel). Because of this fact, the gate voltage no longer controls the channel conductance in the manner stated above equation. The lower boundary on the gate voltage such that this equation is still valid occurs where the channel carrier concentration is just equal to the bulk doping; that is, $p_{channel} = N_D$. This occurs when the intrinsic Fermi level has been bent such that $\phi_s = 2\phi_f$. This subject will be covered in more detail in Saturation region. For a given voltage such that $|V_G| > |V_{th}|$, as the drain voltage is increased in magnitude from zero volts, the drain current increases linearly first, then slows down, and finally tends to level out as $|V_D|$ is made large. The leveling out of the drain current is associated with the pinching off of the channel near the drain. Once the channel has pinched off, the current is said to have saturated at a given level and is then, to a first approximation , independent of drain voltage. Pinchoff occurs because the voltage across the oxide falls below a critical value. The channel IR drop is the factor causing the reduction in electric field. When E_{ox} is decreased to such a that it can not support sufficient mobile charge in a given portion of the channel, then that region decreases to approximately zero thickness and is said to have pinched off. There are two methods for approximating the mathmatical boundary between the triode and saturation regions. The first method involves letting the charge in the channel go to zero. This can be seen mathematically. Because the channel voltage

$$[V_G - V(y)]C = Q_{SS} + Q_D \tag{A.30}$$

is highest at the drain, pinchoff will begin at the drain as $|V_D|$ is increased. V(y) in equation A.30 can thus be replaced by V_D. Rearranging the terms of equqation gives the relationship

$$V_D = V_G - V_P \tag{A.31}$$

where

$$V_P = -(Q_{SS} + Q_D)/C. \tag{A.32}$$

Notice that pinchoff voltage given is exactly the same as the threshold voltages . Equation A.32 states mathematically the boundary line between the triode and saturation regions which is shown plotted in figure. To the right of this line, operation is in the triode region, where $|V_D| < |V_G - V_P|$.

The second method of defining the saturation triode boundary can be found by examining equation for I_d. For a given gate and threshold voltage, the magnitude of the drain current increases as $|V_D|$ is increased from zero volts. Initially, the $(V_G - V_{th})V_D$ term dominates the expression, resulting in the increase of $|I_D|$. Soon, however, the quadratic term becomes significant, with the result that the rate of increase of the current falls off. At some drain voltage, $|I_D|$ will reach a maximum. Past this point, the equation predicts a decrease. However, at the maximum current point, the device has reached saturation and the device model and equations change. This is why a decrease in current is not seen. To find the maximum of $|I_D|$, the expression can be differentiated with respect to the drain voltage and set equal to zero.

Once saturation has been reached, the voltage drop across the inverted portion of the channel tends to remain fixed at $V_G - V_P$, while V_D varies. To a first approximation, this constant voltage across a constant channel resistance results in a constant drain current. Once saturation has been reached , the output characteristics curves can be approximated by horizontal lines. The equation for the current in saturation can be found by placing $V_D = V_G - V_P$ into previous equation for I_d, which results in

$$I_D = -\frac{\beta}{2}(V_G - V_P)^2 \tag{A.33}$$

This equation is valid for

$$|V_D| >= |V_G - V_P|. \tag{A.34}$$

A.4 Ion-implanted Depletion mode devices

Depletion mode MOSFET's are fabricated by introducing impurity ions of the opposite type to the starting substrate to form a shallow layer underneath gate of the device. This layer is most commonly achieved by ion implantation because excellent control of the number of impurity atoms and their distribution is possible to produce an n-channel depletion mode device in a standard NMOS process. N-type of impurities are selectively introduced into the P-type starting material. If an n-doped polysilicon gate is used, the resulting device will have a negative threshold voltage and is capable of conducting current with zero gate to source voltage. For this reason, these devices are typically used in logic circuits where a constant current load is desired.

Appendix B

B.1 Effects Of The DOS On The I-V Characteristics Of POLY-Si TFT

A high DOS results in a slow turn-on of the transfer characteristics. This makes difficult to define a threshold voltage (V_T) and a field effect mobility (μ), since a linear $I_D - V_{GS}$ regime may not be present at all. The apparent threshold voltage (V_T) and mobility (μ) are deduced here from the I_D=0 intercept and slope, respectiviely, of the tangent to the $G - V_{GS}$ curve. The effect of the DOS on the $G - V_{GS}$ characteristics is studied in detail by using the following set of equations,

$$\frac{dG}{d\psi_s} = q\mu_n \frac{n(\psi_s) - n_0}{F_s} \tag{B.1}$$

$$F_s{}^2 = \frac{2q}{\epsilon}\int_{E_v}^{E_c} N(E)H(\psi_s, E, E_F)dE + A\int_{E_c}^{\infty}(E - E_c)^{1/2}H(\psi_s, E, E_F)dE \tag{B.2}$$

$$V_{GS} - V_{FB} = \psi_s + V_{ox} = \psi_s + \frac{t_{ox}}{\epsilon_{ox}}(\epsilon F_s - Q_{ss}) \tag{B.3}$$

N(E), in the upper half of the forbidden gap

$$N(E) = N_T \exp(\frac{E - E_c}{kT_T}) + N_D \exp(\frac{E - E_c}{kT_d}) \tag{B.4}$$

Expression for G,

$$G = \mu_n \frac{\epsilon_{ox}}{t_{ox}}[V_{GS} - V_{FB} - (\psi_s + t_{ox}\frac{Q_{fixed}}{\epsilon_{ox}})] \tag{B.5}$$

The threshold voltage is defined as :

$$V_T = \psi_s + t_{ox}\frac{Q_{fixed}}{\epsilon_{ox}} + V_{FB} \tag{B.6}$$

associated to the grain boundary defects are considered as uniformly distributed over the grain volume. The band bending in the polysilicon is determined by Poisson's equation:

$$\frac{d^2\psi}{dx^2} = \frac{q}{\epsilon}[N_{trap} + n(x) - n_0] \tag{B.10}$$

Where N_{trap} is the net concentration of negatively charged centers, and n(x)-n_0 is the change in electron concentration with respect to equilibrium. These quantities can be written as functions of ψ:

$$N_{trap} = \int_{E_v}^{E_c} N(E)[f(E, E_F + q\psi) - f(E, E_F)]dE \tag{B.11}$$

$$n(\psi) - n_0 = A\int_{E_c}^{\infty} (E - E_c)^{1/2}(f - f_0)dE \tag{B.12}$$

where:

$$A = \frac{2N_c}{\pi^{1/2}kT^{3/2}} \tag{B.13}$$

$$f(E, E_F + q\psi) = [1 + \exp(\frac{E - E_c - q\psi}{kT})]^{-1}, \tag{B.14}$$

and

$$f_0 = f(\psi = 0) \tag{B.15}$$

Multiplying both sides of Equation B.2 by $2\frac{d\psi}{dx}$ and integrating from x=0(oxide/semiconductor interface) to x=d (the unmodulated neutral bulk where $\frac{d\psi}{dx} = 0$)one obtain:

$$F_s{}^2 = \frac{2q}{\epsilon}\int_0^{\psi_s} d\psi \int_{E_v}^{E_c} N(E)[f(E, E_F + q\psi) - f(E, E_F)]dE$$
$$+\frac{2q}{\epsilon}A\int_0^{\psi_s} d\psi \int_{E_c}^{\infty} (E - E_c)^{1/2}[f(E, E_F + q\psi) - f(E, E_F)dE] \tag{B.16}$$

where

$$F_s = -\frac{d\psi}{dx} \tag{B.17}$$

at x=0 is the surface electric field. By changing the order the integration, This equation B.16 is reduces to:

$$F_s{}^2 = \frac{2q}{\epsilon}\int_{E_v}^{E_c} N(E)H(\psi_s, E, E_F)dE$$
$$+\frac{2q.A}{\epsilon}\int_{E_c}^{\infty} (E - E_c)^{1/2}H(\psi_3, E, E_F)dE$$

where

$$H(\psi_s, E, E_F) = \frac{kT}{q}ln(f_0[\exp(\frac{q\psi_s}{kT}) + \exp(\frac{E - E_f}{kT})]) - \psi_s,$$

The conductance G is defined as:

$$G = q\mu_n \int_0^d n(x)dx \tag{B.20}$$

By changing the variable of integration from x to ψ and taking the derivative of the both sides with respect to ψ_s .

$$\frac{dG}{d\psi_s} = q\mu_n \frac{n(\psi_s - n_0}{F_s} \frac{dG}{d\psi_s} = q\mu_0 n_0 \frac{\exp(q\psi_s/kT) - 1}{F_s} \tag{B.21}$$

Gauss's Law can be written as:

$$V_{GS} - V_{FB} = \psi_s + V_{ox} = \psi_s + \frac{t_{ox}}{\epsilon_{ox}}(\epsilon F_s + Q_{ss}) \tag{B.22}$$

Here, Q_{ss} is the charge in the interface states at the oxide/semiconductor interface. This Equation (B.22)is re-written in terms of the fixed charge (Q_{fixed}), by using the relationship:

$$\begin{aligned} F_s &= \frac{1}{\epsilon}\int_0^d (qn(x) + \rho_{sc})dx \\ F_s &= \frac{G}{\epsilon\mu_n} + \frac{1}{\epsilon}\int_0^d \rho_{sc}(x)dx \\ &= \frac{G}{\epsilon\mu_n} + \frac{Q_{sc}}{\epsilon}, \end{aligned} \tag{B.23}$$

B.3 Determination of the DOS by the temperature Method

Taking Equation (B.21), for qψ/kT >> 1, and multiplying both sides by $d\psi_s/V_{GS}$, one obtains:

$$\frac{dG}{dV_G} = \frac{G_0}{d} \frac{\exp(q\psi_s/kT)}{F_s(dV_G/d\psi_s)} \tag{B.24}$$

This indicates that $\psi_s(V_{GS})$ can be deduced from a plot of $\log(dG/d\psi_s)$ vs 1/T.

Appendix C

C.1 Program for MOSFET Model

```
#include <stdio.h>
#include <math.h>
double I_d();
double I1_d();
double vds[25],value;
double a();
double gamma();
double gamma1();
double l_i();
double v_b_s=-3.0;
double v_g_s=5.0;
double v_t=.045;
double theta();
double theta1();
double eta1();
double eta();
double I_d_sat=1.0e-3;
double k();
double W=2.16e-6;
double velocity_l=15.0e4;
double v_d_sat();
double v_c();
double a();
double A();
double B();
double q= 1.6e-19;
double n=1.2e21;
double d=10.0e-9;
double D_j=0.5e-6;
double epsilon_o=8.850e-12;
double epsilon_s_i=12.0;
```

```
double l=13.4e-6;
int i;
double v_t2=4.0e-2;
double v_t1=8.0e-2;
double phi_f=0.3;
double v_b_s2=-8.0;
double v_b_s1=-1.5;
double gamma_0=49.5e-6,t_o_x=0.045e-6;



double I_d(i)
int i;
{
double I_d;
/*printf("@@@@%lf\n",vds[i]);*/
if((vds[i]>=0 && vds[i]<v_d_sat()) && v_g_s >=v_t)
{
I_d= gamma(i)*W*(v_g_s-v_t-a()*vds[i]/2.0)*vds[i]/l;
/*printf("!\t%lf\n",gamma(i));
printf("5\t%lf\n",W);
printf("t\t%lf\n",v_g_s);
printf("r\t%lf\n",v_d_s);
printf("r\t%lf\n",v_t);
printf("r\t%lf\n",a());
printf("r\t%lf\n",v_d_s);*/
/*printf("I_d=%lf\n",I_d);*/
}
else if(vds[i]>v_d_sat() && v_g_s>=v_t)
{
 I_d=gamma(i)*W*(v_g_s-v_t-a()*v_d_sat()/2.0)*v_d_sat()/l_i(i);
/*printf("ganma!\t%lf\n",gamma());
printf("W\t%lf\n",W);
```

```
printf("v_g_s\t%lf\n",v_g_s);
printf("v_d_s\t%lf\n",v_d_s);
printf("v_t\t%lf\n",v_t);
printf("a\t%lf\n",a());
printf("v_d_sat()\t%lf\n",v_d_sat());
printf("l_i()\t%lf\n",l_i());*/
/*printf("I_d=%lf\n",I_d);*/
}
else if (v_g_s<v_t)
{
I_d=0.0;
/*printf("I_d=%lf\n",I_d);*/
}return I_d;
}


double mu_o(gamma_0,t_o_x)
double gamma_0,t_o_x;
{
double epsilon_o=8.85e-12;
double epsilon_o_x=3.9;
return (gamma_0*t_o_x)/(epsilon_o*epsilon_o_x);
return ;
}


double  v_c()

{
return (velocity_l*l/mu_o(49.5e-6,0.045e-6));
/*printf("v_c\t%lf\n",v_c());

printf("mu_o\t%lf\n",mu_o(49.5,0.045e-6));
```

```
        printf("velocity_1\t%lf\n",velocity_1);
printf("length\t%lf\n",l);
*/
}
double k()

{
return (v_t2-v_t1)/(sqrt(2.0*phi_f-v_b_s2)-sqrt(2.0*phi_f-v_b_s1));
}

double v_d_sat()
{
double V_ds,sum1,sum2,sum3;
sum1=v_g_s-v_t;
sum1=sum1/1.0;
sum2=v_c();
sum3=sum1*sum1+v_c()*v_c();
sum3=sqrt(sum3);
V_ds=(((v_g_s-v_t)/a())+v_c())-sqrt(((v_g_s-v_t)*(v_g_s-v_t)/pow(a(),2.0))
+(pow(v_c(),2.0)));
V_ds=sum1+sum2-sum3;
/*printf("V_Dstaurated=\t%lf\n",V_ds);*/

return V_ds;
}



double a()


{
double temp=0.0;
```

```
temp=1.0;
        temp+=0.5*k()*(1.0 - 1.0/(1.41 +0.43*(2.0*phi_f - v_b_s)))/
sqrt(2.0*phi_f-v_b_s);
return temp;
}


double gamma(i)
int i;
{
double gamma_0=49.5e-6;
double t;

/*printf("##%f\n",vds[i]);*/
t =(gamma_0/(1.0+theta()*(v_g_s-v_t-vds[i]/2.0+k()*sqrt(2.0*phi_f-v_b_s))+
eta()*vds[i]));
/*printf("%lf\n",t);*/
return  t;
}




double theta()
{
double theta_0=0.055;
double theta_1=0.004e-6;
/*printf("theta=%lf\n",theta_0+theta_1/l);*/
return theta_0+theta_1/l;
}
```

```
double eta()
{
double eta_0=0.008;
double eta_1=0.25e-6;
/*printf("eta=%lf\n",eta_0+eta_1/l);*/
return eta_0+eta_1/l;
}
```

```
double l_i(i)
int i;
{
return l-l*(sqrt(pow(v_c(),2.0)+2.0*A()*(1.0+B()*I_d_sat)*(vds[i]-v_d_sat()))-
/(A()*(1.0+B()*I_d_sat));
}
double A()
{
return q*n*l*l/(epsilon_o*epsilon_s_i);
}
double B()
{
return 2.0*(log(D_j/d)-1.0)/(q*n*velocity_l*W*D_j);
}
```

```
double gamma1()
{
double gamma1_0=49.5e-6;

return gamma1_0/(1.0+theta1()*(v_g_s-v_t-vds[i]/2.0+k()*sqrt(2.0*phi_f-v_b_s))+eta1()*v
}
double theta1()
{
double theta_0=0.055;
double theta_1=0.004e-6;
return theta_0+theta_1/l_i(i);
}
double eta1()
{
double eta_0=0.008;
double eta_1=0.25e-6;
return eta_0+eta_1/l_i(i);
}
```

```
main()
{
int i;
        FILE *data;
data=fopen("data.dat_.055_5","w");
printf("the saturated_voltage=\t%lf\n",v_d_sat());
printf("enter 25 real numbers\n");
for(i=0;i<25;i++)
```

```
{
scanf("%lf",&value);
vds[i]=value;
}
/*printf("PLEASE ENTER v_t,v_g_s,v_d_s, threshold voltage,voltage_drain_sourc
voltage_gate_source\n");
scanf("%lf%lf%lf",&v_t,&v_g_s,&vds);*/
/*   printf("the gamma=\t%lf\n",gamma(i));
printf("the v_c=\t%lf\n",v_c());*/

for(i=0;i<25;i++)
{
fprintf(data,"%lf\t%lf\n",vds[i],I_d(i));
printf("vds=%lf\n",i,vds[i]);
printf("I_d[%d]=%lf\n",i,I_d(i));
/*        I_d(i);*/
}
printf("\n");
fclose(data);
}
```

C.2 Program For The Subthreshold Characteristics Of Poly-Si TFT's

```
#include <math.h>
#include <stdio.h>
double y();
double x;
double g_0();
double epsilon_ox=3.9;
double t_ox=0.1e-6;
double n_t();
double n_c=1.3e25;
/*double n_c=3.2e25;*/
double (e_fec)=-0.42;
double mu=5e-4;
double q=1.6e-19;
double t;
double v_g;
double k=(69.0e-3)/800.0;
double k_0();
double G();
double t_g=800.0;
double v_0();
double k_tg=(69.0e-3);
double n_g=3.0e26;
double d=0.6e-6;
double f();
double epsilon_0=8.85e-12;
double epsilon_s=11.9;
  double y()
{
return log10(g_0()*epsilon_ox*epsilon_0/(n_t()*d*t_ox))+(2.0*t_g/t-2.0)*(log1
-log10(v_0()));
```

```
}
double f()
{
return sqrt(2.0*n_t()*k_tg*q/(epsilon_s*epsilon_0));
}
double n_t()
{
return n_g*k_tg*exp((e_fec)/(k_tg));
}
double g_0()
{
return mu*d*n_c*exp((e_fec)/(k*t));
}
double v_0()
{
return epsilon_s*t_ox*f()/epsilon_ox;
}
double G()
{
return g_0()+k_0()*pow(x,2.0*t_g/t-1.0);
}
double k_0()
{
return q*mu*n_c*(t/(2.0*t_g-t))*pow(2.0*epsilon_s*epsilon_0/(n_g*pow(q,2.0)),0.
pow(pow(epsilon_ox,2.0)/(2.0*epsilon_s*epsilon_0*pow(t_ox,2.0)*(n_g/q)*pow(k*q,
pow(t_g,2.0)),2.0*t_g/t-1.0/2.0);
}
main()
{
int i;
FILE *data;
data=fopen("a.dtft4","w");
for (i=0;i<12;i++)
```

```
{

/*printf("Please Enter x,t\n");
scanf("%lf%lf",&x,&t);*/
printf("Please Enter v_g,t\n");
scanf("%lf%lf",&v_g,&t);
printf("y=\t%lf\n",y(x));
printf("x=\t%lf\n",x);
printf("x_2=\t%lf\n",x*x);
printf("t=\t%lf\n",t);
printf("f=\t%lf\n",f());
printf("n=\t%lf\n",n_t());
printf("g=\t%lf\n",g_0());
printf("v=\t%lf\n",v_0());
printf("k=\t%lf\n",k_tg);
printf("n_g=\t%lf\n",n_g);
printf("n_c=\t%lf\n",n_c);
printf("e_f=\t%lf\n",e_fec);
printf("%f\t%lf\n",(x*x),pow(10,y()));
/*fprintf(data,"%f\t%lf\n",log10(x*x),y());*/
/*fprintf(data,"%f\t%lf\n",log10(x),y());*/
fprintf(data,"%f\t%lf\n",log(G()),v_g);
}
fclose(data);
}
```

C.3 Program For Accumulation Mode Of Poly-Si TFT'

```
#include <stdio.h>
#include<math.h>
double mu_b=11.0e-4;
double q=1.6e-19;
double mu();
double psi();
double W=10.0e-6;
double L=10.0e-6;
double psi_0=0.55;
double alpha();
double I();
double V_d=0.5;
double V_g;
double N_st=2.1e16;
double epsilon=8.85e-12;
double C_ox=12.0*(8.85e-12)/(78.0e-9);
/*double C_ox=12.0*(8.85e-12)/(78.0e-9)=.0013615385;*/
double d=10.0e-9;
double V_th=1.2;
double k=(8.614e-5)*(1.6e-19);
/*double k=(8.614e-5)*(1.6e-19)=1.37824e-23;*/
double T=300.0;
void input_variables()
{
printf("ENTER V_g\n");
scanf("%lf",&V_g);
}
double mu()
{
return mu_b*exp(-q*psi()/(k*T));
}
double psi()
```

```
{
return alpha()/(V_g-V_th+alpha()/psi_0);
}
double alpha()
{
return q*q*N_st*N_st*d/(8.0*epsilon*C_ox);
}
double I()
{
return (W/L)*C_ox*mu()*((V_g-V_th)*V_d-pow(V_d,2.0)/2.0);
}
main()
{
int i;
FILE *data;
data=fopen("data.datanu1i3","w");
for(i=0;i<25;i++)
{
input_variables();
printf("p=\t%e\n",psi());
printf("v=\t%lf\n",V_g);
printf("c=\t%lf\n",C_ox);
printf("k=\t%e\n",k);
printf("kT=\t%e\n",k*T);
printf("ex=\t%e\n",exp(-q*psi()/(k*T)));
printf("q=\t%e\n",q*q);
printf("I=\t%e\n",I());
printf("q1=\t%e\n",q*N_st);
printf("V_=\t%e\n",pow(V_d,2.0));
printf("a=\t%e\n",alpha());
printf("m=\t%e\n",mu());
printf("m1\t%lf\n",mu());
fprintf(data,"%e\t%e\n",V_g,I());
```

```
}
fclose(data);
}
```

Bibliography

[1] Y P. Tsividis, Operation & Modelling of The MOS Transistor. McGrawHill, New York, 1987

[2] S M. Sze, Physics of Semiconductor Devices. Wiley Eastern Limited, India, 1983.

[3] A.S. Grove, Physics and Technology of Semiconductor Devices. New York, 1967.

[4] Hanafi, Lovell H. Camnitz, and Anthony J. Dally, "An accurate and Simple MOSFET Model for Computer-Aided Design,"IEEE Journal of Solid state circuits , Vol,SC-17, No. 5, OCTOBER 1982(882).

[5] R.H.Crawford, MOSFET in circuit design New York ; Mc-Graw Hill 1967, pp21-23.

[6]J.R.Schriefier, "Effective Carrier mobility in surface space charge layers," Phys.Rev., Vol.97, pp641-649, 1955

[7]G Fortunato, D.B.Meakin and P. Migliorato,"The subthreshold characteristics of polysilicon Thin Film Transistors",J.J.Appl.Phys, Vol. 27 No.11, pp.2124-27.

[8] S.Khisida, Y.Naruke, Yasutaka and M. Matusumura, "Theoretical analysis of amorphous-silicon Field-Effect Transistors" J.J.Appl.Phys. Vol.22, No.3, March, 1983 pp.511-517.

[9] G.Merkel, J.Borel and N.Z.Cupea, " An accurate large signal MOS transistor model for use in computer aided design," IEEE Trans. Electron devices, Vol. ED-19, May 1972.

[10] Tadashi Serikawa.S.Shirai, A.Okamoto, and S.Suyama, "A model of current-voltage characteristics in Polycrystalline Silicon Thin-Film Transistors," IEEE Tras. On Electron Devices, Vol. ED-34, No. 2, FEBRUARY 1987(321).

[11] Migliorato 1989, ~~Courtesy of Academic Press.~~

[12] S W. Kang, K.-S. Min, and K. Lee, "Parametric expression of subthreshold slope using threshold voltage parameters for MOSFET statistical modelling," IEEE Trans. Electron Devices, vol. 43, pp.1382-1386,1996.

[13] G. Fortunato and P. Migliorato, "Determination of gap state density in Poly-Si by field effect conductance". Appl. Phys. Lett. 49 (16), oct 1986.

[14]S.S Ahmed, D.M.Kim, and H. Shichijo, "Modelling of accumulation-mode MOSFET's in polysilicon thin films," IEEE Electron Devices Letts.,Vol.EDL-6, pp.313-3 5, 1985.

[15]J.C. Anderson,"Theory of Thin film transistors," Thin solid films, vol.38, pp. 151-161, 1976.

[16] H. Baudrand, E.Hamadto, and J.L. Amarlic, "An experimental and therotical study of polycrystalline thin film transistors," Solid state electron, Vol.24, pp. 1093-1098, 1982.

[17] Z.H. Liu, C. Hu, J.H. Huang, T. Y. Chan, M. C. Jeng, P. K. Ko, and Y. C. Cheng, " Threshold voltage model for deep-submicrometer MOSFET's," IEEE Trans. Electron Devices, Vol. 40, pp. 86-95,1993.

[18] C. W. Wu and E.S. yang, "physical basis of scattering potential at grain boundary of polysilicon semiconductors,"Appl.Phys. Lett., vol. 40, pp.49-51, 1982.

[19] J.G.Fossum, Fellow, IEEE and Adelmo Ortiz-Conde, Student member, IEEE, " Effects of grain boundaries on the channel conductance of SOI MOSFET's", IEEE Trans. on electron devices, Vol.ED-30, No.8, Aug. 1983.

[20] H. F. Matare, "Carrier transport at grain boundaries in semiconductors," J. appl. Phys., vol. 56, pp. 2605-2631, 1984.

[21] M.Shur, M.Hack, "An analytical model for amorphous silicon thin film transistors," J.Appl.Phys., Vol.66, pp. 3371-3380, Oct 1989.

[22] G. Baccarani and B. Ricco,"Transport properties of polycrystalline silicon films", J.Appl.Phys. 1978.

[23] G. Baum and H. Reneking, "Drift velocity saturation in MOS transistors, " IEEE Trans. Electron Devices, vol. ED-17, PP.481-182, June 1970.